

SERVICE MANUAL

COLOUR TELEVISION 90°

CHASSIS F-10

CHASSIS F-12

CHASSIS F-14

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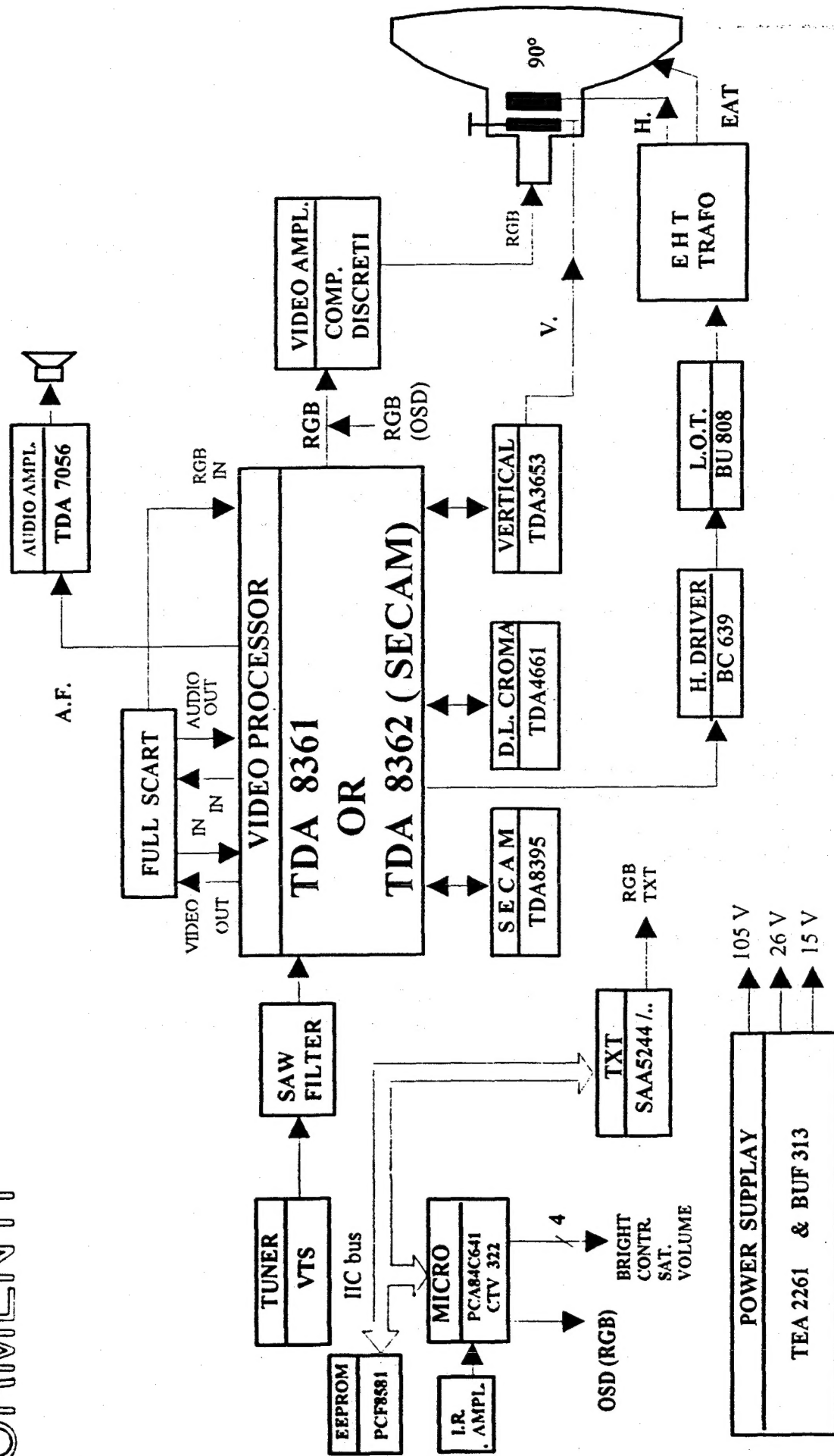
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FORMENTI



F10 BLOCK DIAGRAM

CHASSIS F-10 INTRODUCTION

The television is built around a high-volume integration integrated circuit TDA 8361/2, a new processor for PAL and NTSC system television.

This TDA 8361/2 processor combines all the small signal functions required of a colour television receiver, including operation of an external video and audio of a S-VHS (separate Luminance and Chrominance).

Processor TDA 8361/2 is a video processor containing functions handling HF, sound, Horizontal and vertical synchronisation, PAL/NTSC decoding, and RGB control. It was implemented using BIMOS technology, which combines MOS and bipolar methods. The bipolar technology is used for high-frequency signal processing (ex. video signals) and the MOS technology is used in those parts handling digital signals.

In addition it uses an integrated delay line TDA 4661, an audio output stage TDA 7056, a vertical output stage TDA 3653B, and a horizontal output stage with Darlington BU 808D. The power-supply unit is of the flyback type and controlled by the TEA 2261 integrated circuit.

Principal functions common to both processor version TDA 8361/2 are :

- symmetric IF amplifier directly coupled to surface-wave filter
- FM sound multistandard demodulator, not needing regulation
- chroma trap and integrated band-pass filters
- integrated luminance delay line
- PAL/NTSC automatic decoder
- self-regulating horizontal oscillator
- low dissipation (about 700 mW)
- possibility of selecting an external A/V source

Functions specific to TDA 8362 :

- multistandard IF circuit for positive and negative modulation
- simple interface with TDA 8395 (SECAM decoder) for PAL and SECAM multistandard applications.

CHASSIS F-10 ALIGNMENTS

38.9 MHz and AFC (TP2)

Connect a 38.9 MHz intermediate-frequency generator to the tuner's IF output pin 17 and adjust the core L3 so as to obtain 4 V. at pin 44 of TDA 8361/2 (in order to obtain a voltage of about 2.5 V. at the terminals of divided R 129 and R 128 - pin 9 of tuning integrated-circuit).

POWER SUPPLY (TP3)

Measure the direct voltage at the terminals of capacitor C 111 and potentiometer VR 9 so as to obtain a voltage of 105 V (110 V for 21").

AGC (TP1)

Apply a 60dBuV (+/- 1 dB) RF signal, band III, channel 10-to-12, and adjust potentiometer VR7 so as to obtain a voltage of about 8 V at tuner pin no. 5. (This voltage depends on the tuner used; so check on the latter's characteristics.)

WHITE SETTING

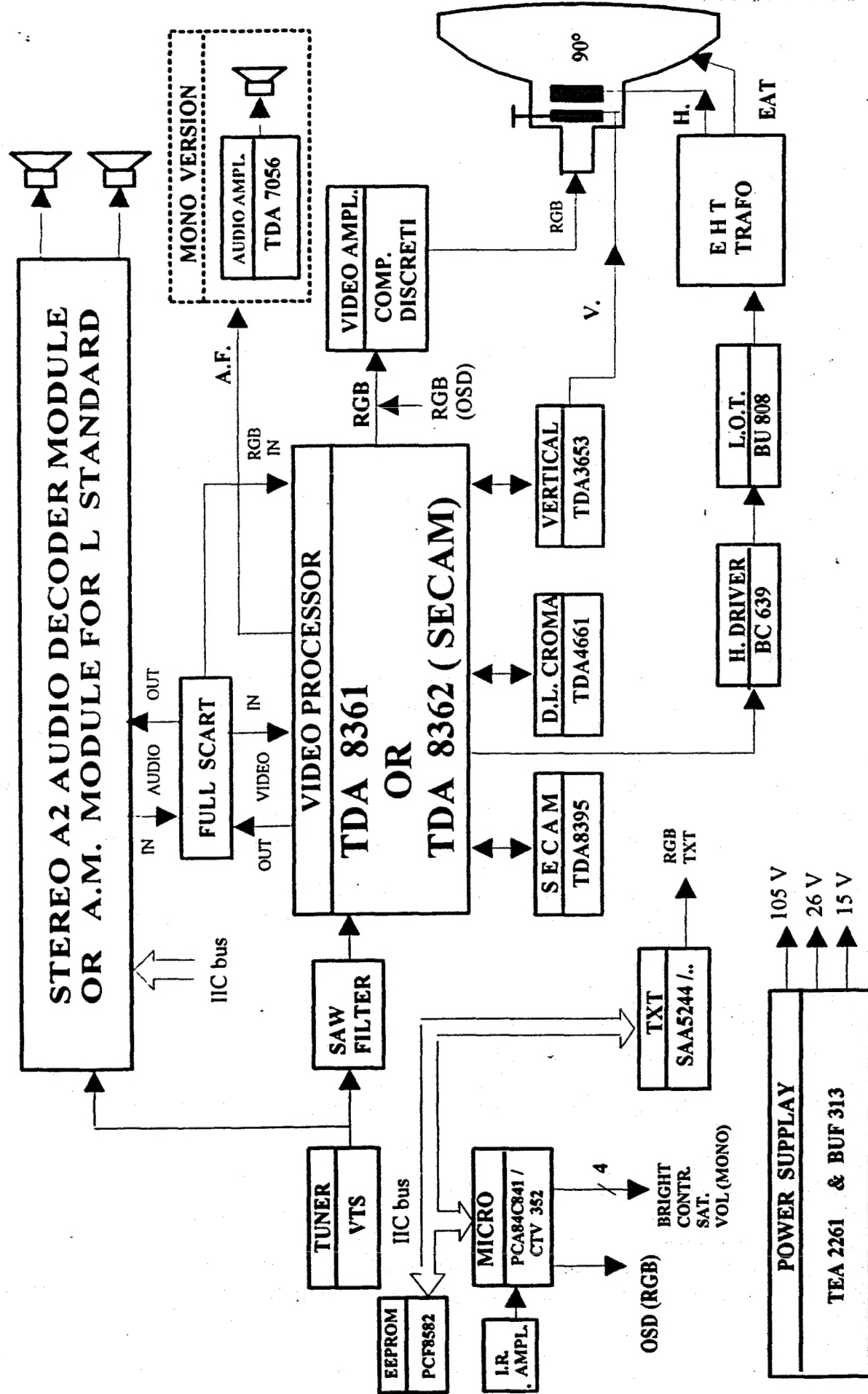
- Tune to a channel with colour test-pattern signal
- Position level potentiometers RL, GL, BL, and gain potentiometers RG and BG on the CRT socket, locating centrally
- Adjust the TV receiver to maximum brightness, minimum colour and contrast
- Switch the TV to AV using the corresponding button on the remote control
- Adjust potentiometer G2 (EHT transformer) to obtain a barely visible screen. The screen usually appears with a predominant colour hue.
- Adjust the level potentiometers of the order two cathodes that are different from the predominant colour in order to obtain the white screen. If, for example, the predominant colour of the screen is red, the potentiometers of the blue cathode BL and the green cathode GL are adjusted.
- Return to the TV mode with the appropriate remote-control button.
- Check that the hue of the colours of the colour test-pattern picture are correct. If necessary adjust the potentiometers RG-BG.

VERTICAL CENTERING

- Adjust VR 10 (VA) for proper vertical height
 - Adjust VR 11 (VL) for proper vertical linearity
- Cut/solder the jumpers JS22 and/or JS23 in order to obtain the right vertical geometric centering between CRT and signal. (for example, use a test-pattern signal)

4.43 MHz SETTING

- Apply a PAL colour-bar signal to the antenna
 - Adjust pin 26 of TDA 8361/2 to the voltage of 8 V. (in these conditions the phase detector and the killer circuit are disabled)
 - Set variable capacitor 2/20 pf C72 to obtain the minimum colour flicker.
- Note : capacitor C72 is usually a fixed condenser of adequate value set for the minimum flicker.



F12 BLOCK DIAGRAM

CHASSIS F-12 INTRODUCTION

The television is built around a high-volume integration integrated circuit TDA 8361/2, a new processor for PAL and NTSC system television.

This TDA 8361/2 processor combines all the small signal functions required of a colour television receiver, including operation of an external video and audio of a S-VHS (separate Luminance and Chrominance). Processor TDA 8361/2 is a video processor containing functions handling HF, sound, Horizontal and vertical synchronisation, PAL/NTSC decoding, and RGB control. IT was implemented using BIMOS technology, which combines MOS and bipolar methods. The bipolar technology is used for high-frequency signal processing (ex. video signals) and the MOS technology is used in those parts handling digital signals. In addition it uses an integrated delay line TDA 4661, 2 audio output stages each using TDA 7056, a vertical output stage TDA 3653B, and a horizontal output stage with Darlington BU 808D. The power supply unit is of the flyback type and controlled by the TEA 2261 integrated circuit.

Principal functions common to both processor version TDA 8361/2 are :

- symmetric IF amplifier directly coupled to surface-wave filter
- FM sound multistandard demodulator, not needing regulation
- chroma trap and integrated band-pass filters
- integrated luminance delay line
- PAL/NTSC automatic decoder
- self-regulating horizontal oscillator
- low dissipation (about 700mW)
- possibility of selecting an external A/V source

Functions specific to TDA 8362 :

- multistandard IF circuit for positive and negative modulation
- simple interface with TDA 8395 (SECAM decoder) for PAL and SECAM multistandard applications.

Stereo decoder module

The stereo decoder module is connected to the F 11 chassis through the S connector (side of the tuner) . From the connector, + 12 V. supply (pin S 6) voltage is applied to the module. From the same connector S at pin S 9 and S 13, AUDIO OUT signal is sent to the scart connector, whereas AUDIO IN is sent from the scart connector to module through pins S 12 and S 14. SDA and SCL control signals from the uP passes through pins S 1 and S 2 to the module. The module receives the intercarrier signal (coaxial cable) and the + 16 V supply voltage for the audio output stages through the connector CN 3. The intercarrier signal is filtered by two audio filters 5.5 MHz and 5 74 MHz. It is demodulated by IC 1 (TDA 9821). The two audio output signals from the demodulator are elaborated by the audio processor IC 2 (TDA 9840), which identifies the type of demodulated audio signal and switches the audio signal for output to the SCART connector. The adjustments of volume, balance and tones are carried out by IC 3 (TDA 8425). All the adjustments are done through the i2cbus, just as the transfer of information to the uP for the management of OSD. The +5 V supply for IC 1 and IC 2 is obtained from the +12 V supply using the IC 4 (L 7805) regulator. The audio output signal from IC 3 is sent to the final audio IC 5 and IC 6 (TDA 7056) for power amplification.

CHASSIS F-12 ALIGNMENTS

38.9 MHz and AFC

Connect a 38.9 MHz intermediate-frequency generator to the tuner's IF output pin 17 and adjust the core L 3 so as to obtain 4 V. at pin 44 of TDA 8361/2 (in order to obtain a voltage of about 2.5 V. at the terminals of divided R 129 and R 128 - pin 9 of tuning integrated-circuit).

POWER SUPPLY

Measure the direct voltage at the terminals of capacitor C 111 and potentiometer VR 9 so as to obtain of 105V (110V for 21").

AGC

Apply a 60dBuV (+/- 1 dB) RF signal, band III, channel 10-to-12, and adjust potentiometer VR7 so as obtain a voltage of about 8 V at tuner pin no. 5 .

WHITE SETTING

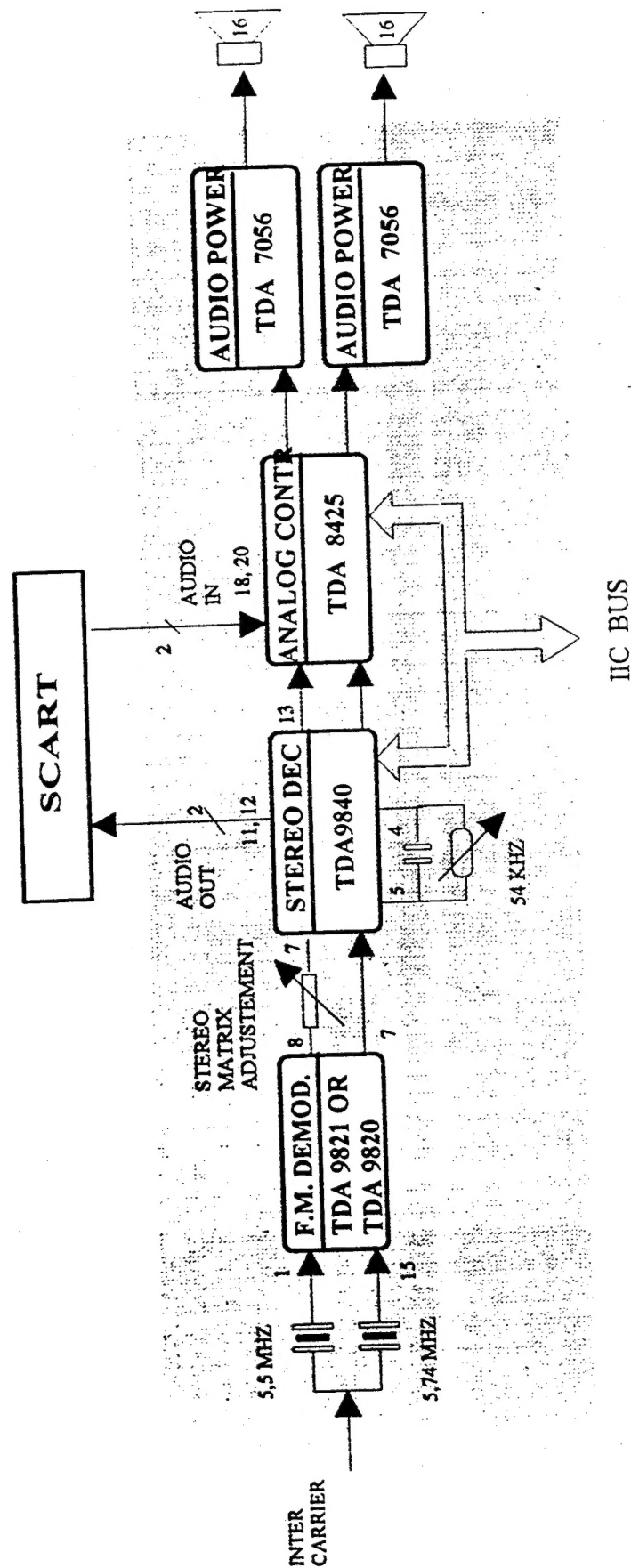
- Tune to a channel with colour test-pattern signal
- Position level potentiometers RL, GL, BL, and gain potentiometers RG and BG on the CRT socket, locating centrally
- Adjust the TV receiver to maximum brightness, minimum colour and contrast
- Switch the TV to AV using the corresponding button on the remote control
- Adjust potentiometer G2 (EHT transformer) to obtain a barely visible screen. The screen usually appears with a predominant colour hue
- Adjust the level potentiometers of the order two cathodes that are different from the predominant colour in order to obtain the white screen. If, for example, the predominant colour of the screen is red, the potentiometers of the blue cathode BL and the green cathode GL are adjusted.
- Return to the TV mode with the appropriate remote-control button.
- Check that the hue of the colours of the colour test-pattern picture are correct. If necessary adjust the potentiometers RG-BG.

VERTICAL CENTERING

- Adjust VR 10 (VA) for proper vertical height
 - Adjust VR 11 (VL) for proper vertical linearity
- Cut/solder the jumpers JS22 and/or JS23 in order to obtain the right vertical geometric centering between CRT and signal. (For example, use a test-pattern signal).

4.43 MHz SETTING

- Apply a PAL colour-bar signal to the antenna
 - Adjust pin 26 of TDA 8361/2 to the voltage of 8 V. (in these conditions the phase detector and the killer circuit are disabled).
 - Set variable capacitor 2/20 pf C72 to obtain the minimum colour flicker.
- Note : capacitor C72 is usually a fixed condenser of adequate value set for the minimum flicker.



F12 STEREO MODULE

ALIGNMENT STEREO MODULE

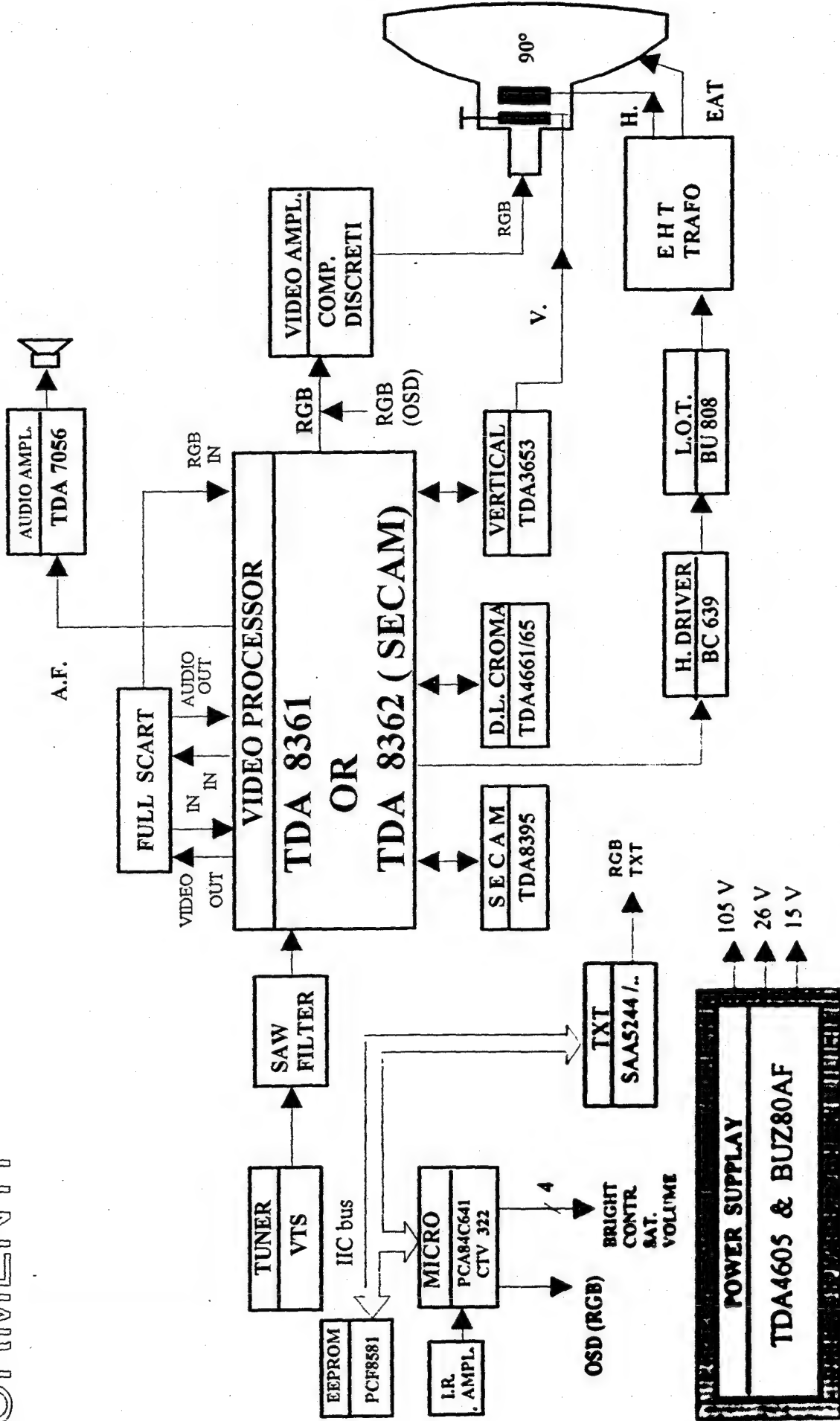
Insert the stereo module in connector "S" of the chassis and insert the intercarrier signal connector CN 3 .
Apply to the CTV antenna input connector a TV signal with audio stereo ($R = 3 \text{ KHz}$ $L = 1 \text{ KHz}$) from a generator, or alternatively, tune to a TV channel with stereo transmission. Adjust the coil L 1 to obtain the maximum level of signal at IC 2 pin 5.

ADJUSTMENT OF VR 1 (STEREO DEMATRIXING) .

For this adjustment only stereo signal from generator should be used.

Connect the probe scope at pin 1 and 3 of IC 3. Eliminate modulation tone of the left channel, adjust the trimmer VR1 for the minimum level of signal on the right channel (pin 1 of IC 3).

Bilingual decoding : is verified using a TV generator in a dual mode or tuning a TV channel with bilingual program, verify the switching of the language by A/B button on the remote control and check the relative OSD.



F14 BLOCK DIAGRAM

CHASSIS F-14 INTRODUCTION

The television is built around a high-volume integration integrated circuit TDA 8361/2, a new processor for PAL and NTSC system television.

This TDA 8361/2 processor combines all the small signal functions required of a colour television receiver, including operation of an external video and audio of a S-VHS (separate Luminance and Chrominance). Processor TDA 8361/2 is a video processor containing functions handling HF, sound, Horizontal and vertical synchronisation, PAL/NTSC decoding, and RGB control. IT was implemented using BIMOS technology, which combines MOS and bipolar methods. The bipolar technology is used for high-frequency signal processing (ex. video signals) and the MOS technology is used in those parts handling digital signals.

In addition it uses an integrated delay line TDA 4661/4665, an audio output stage TDA 7056, a vertical output stage TDA 3653B, and a horizontal output stage with Darlington BU 808D. The power supply unit is of the flyback type and controlled by the TDA 4605 integrated circuit and using a mosfet BUZ80AF.

Principal functions common to both processor version TDA 8361/2 are :

- symmetric IF amplifier directly coupled to surface-wave filter
- FM sound multistandard demodulator, not needing regulation
- chroma trap and integrated band-pass filters
- integrated luminance delay line
- PAL/NTSC automatic decoder
- self-regulating horizontal oscillator
- low dissipation (about 700mW)
- possibility of selecting an external A/V source

Functions specific to TDA 8362 :

- multistandard IF circuit for positive and negative modulation
- simple interface with TDA 8395 (SECAM decoder) for PAL and SECAM multistandard applications.

CHASSIS F-14 ALIGNMENTS

38.9 MHz and AFC

Connect a 38.9 MHz intermediate-frequency generator to the tuner's IF output pin 17 and adjust the core L 3 so as to obtain 4 V. at pin 44 of TDA 8361/2 (in order to obtain a voltage of about 2.5 V. at the terminals of divided R 129 and R 128 - pin 9 of tuning integrated-circuit).

POWER SUPPLY

Measure the direct voltage at the terminals of capacitor C 111 and potentiometer VR 9 so as to obtain of 105V.

AGC

Apply a 60dBuV (+/- 1 dB) RF signal, band III, channel 10-to-12, and adjust potentiometer VR7 so as obtain a voltage of about 8 V at tuner pin no. 5 .

WHITE SETTING

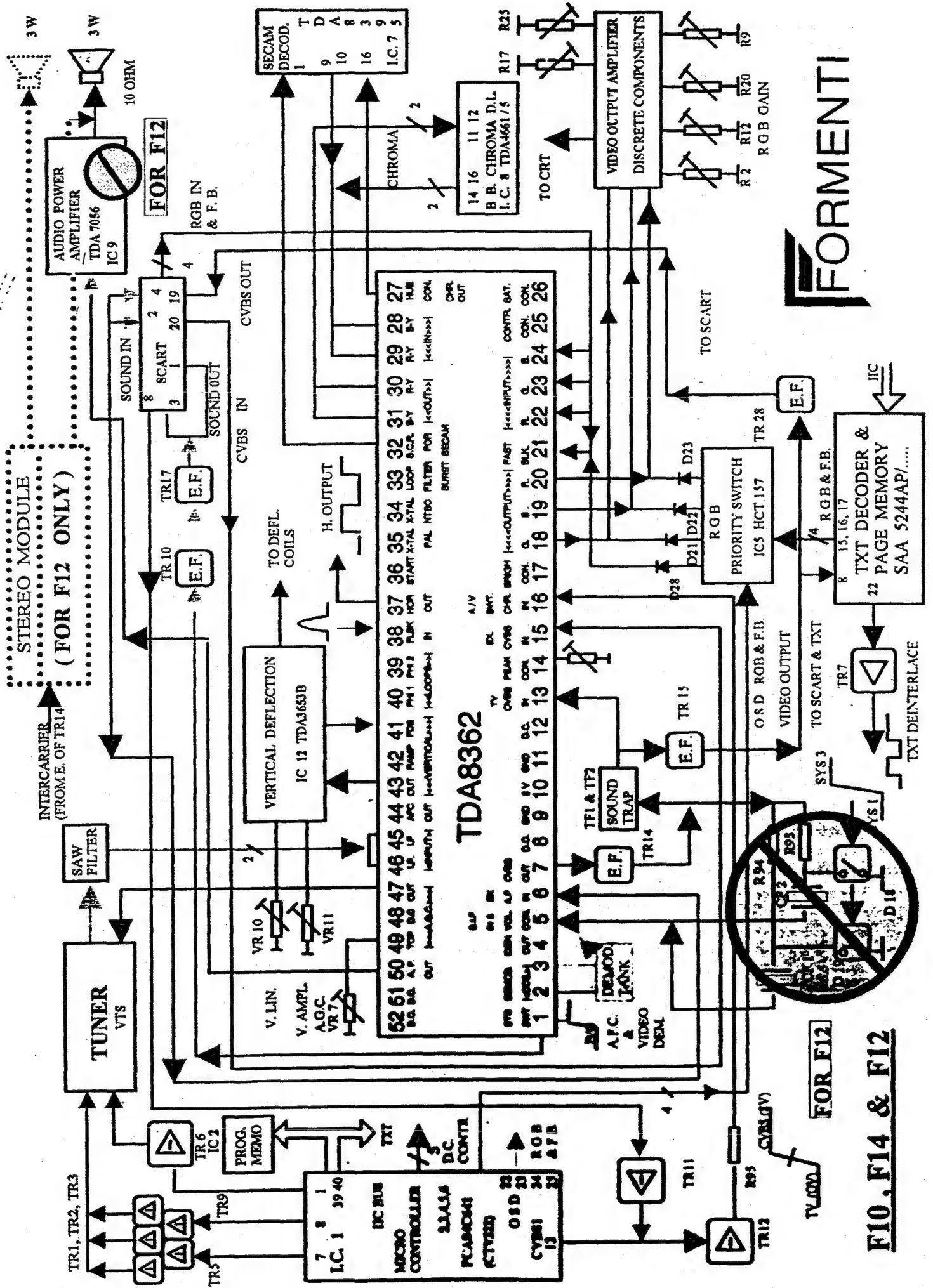
- Tune to a channel with colour test-pattern signal
- Position level potentiometers RL, GL, BL, and gain potentiometers RG and BG on the CRT socket, locating centrally
- Adjust the TV receiver to maximum brightness, minimum colour and contrast
- Switch the TV to AV using the corresponding button on the remote control
- Adjust potentiometer G2 (EHT transformer) to obtain a barely visible screen. The screen usually appears with a predominant colour hue
- Adjust the level potentiometers of the order two cathodes that are different from the predominant colour in order to obtain the white screen. If, for example, the predominant colour of the screen is red, the potentiometers of the blue cathode BL and the green cathode GL are adjusted.
- Return to the TV mode with the appropriate remote-control button.
- Check that the hue of the colours of the colour test-pattern picture are correct. If necessary adjust the potentiometers RG-BG.

VERTICAL CENTERING

- Adjust VR 10 (VA) for proper vertical height
 - Adjust VR 11 (VL) for proper vertical linearity
- Cut/solder R. 200 and/or R. 201 in order to obtain the right vertical geometric centering between CRT and signal. (For example, use a test-pattern signal).

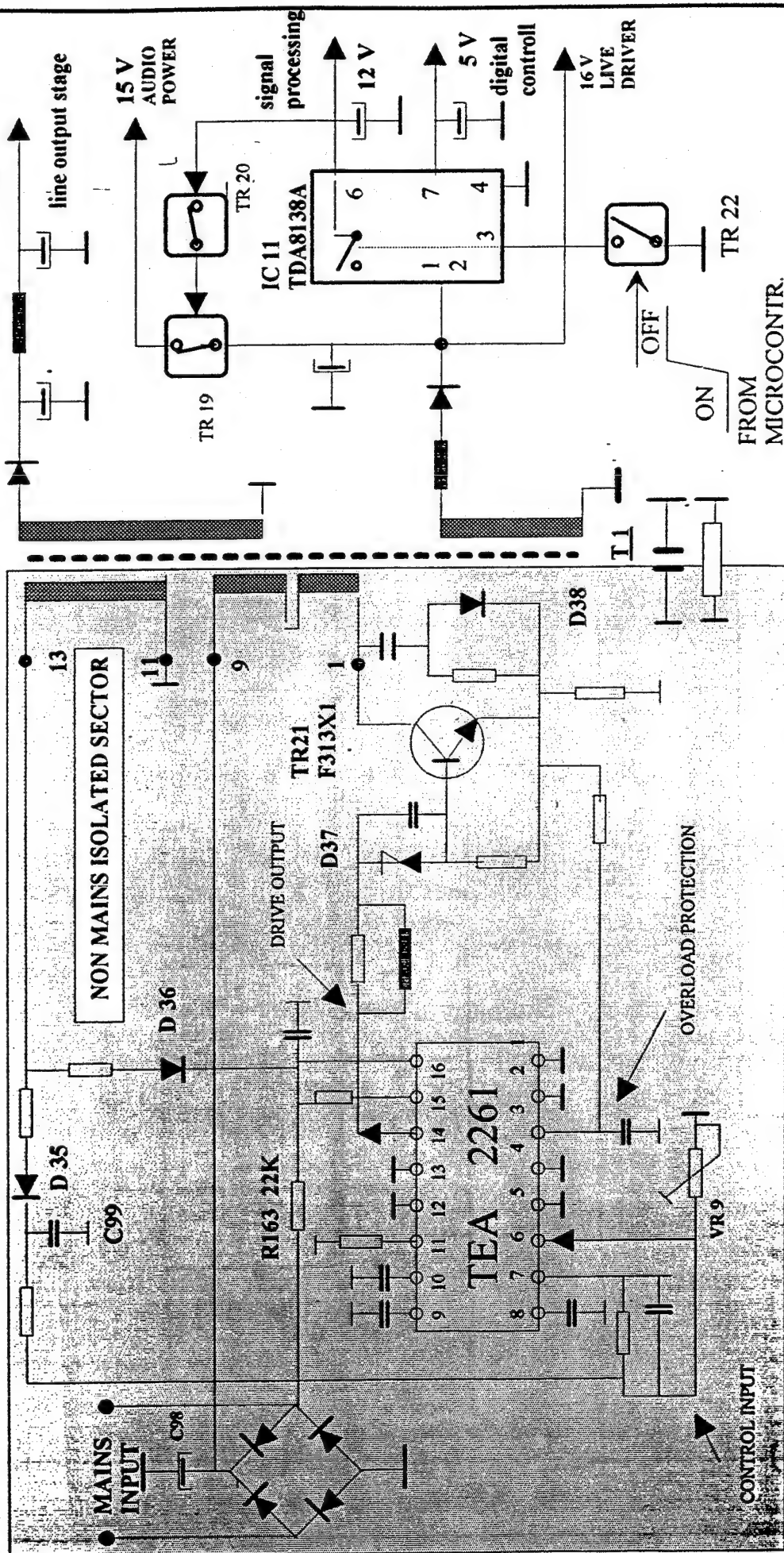
4.43 MHz SETTING

- Apply a PAL colour-bar signal to the antenna
 - Adjust pin 26 of TDA 8361/2 to the voltage of 8 V. (in these conditions the phase detector and the killer circuit are disabled).
 - Set variable capacitor 2/20 pf C72 to obtain the minimum colour flicker.
- Note : capacitor C72 is usually a fixed condenser of adequate value set for the minimum flicker.



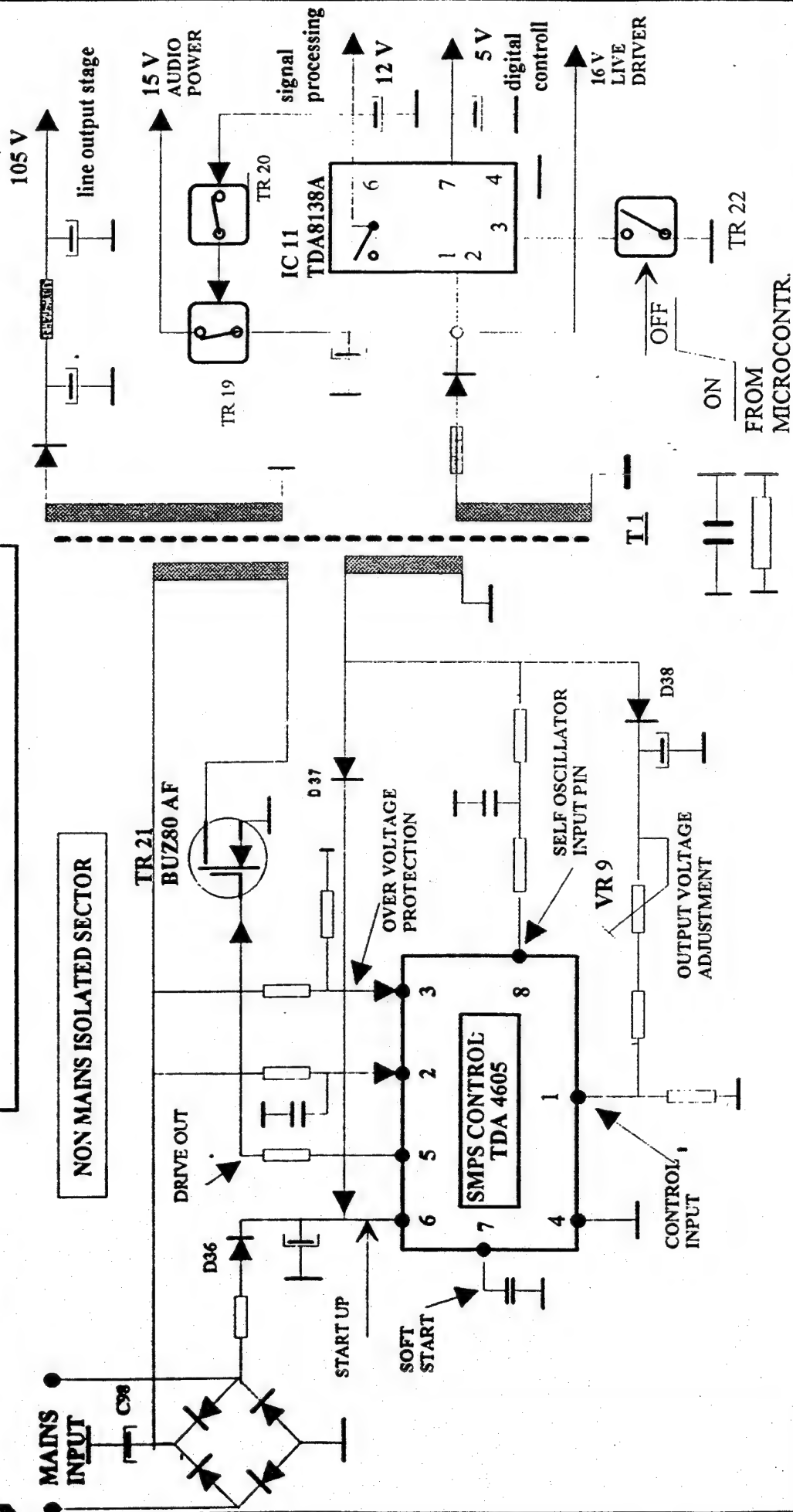
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F10 / F12 POWER SUPPLY



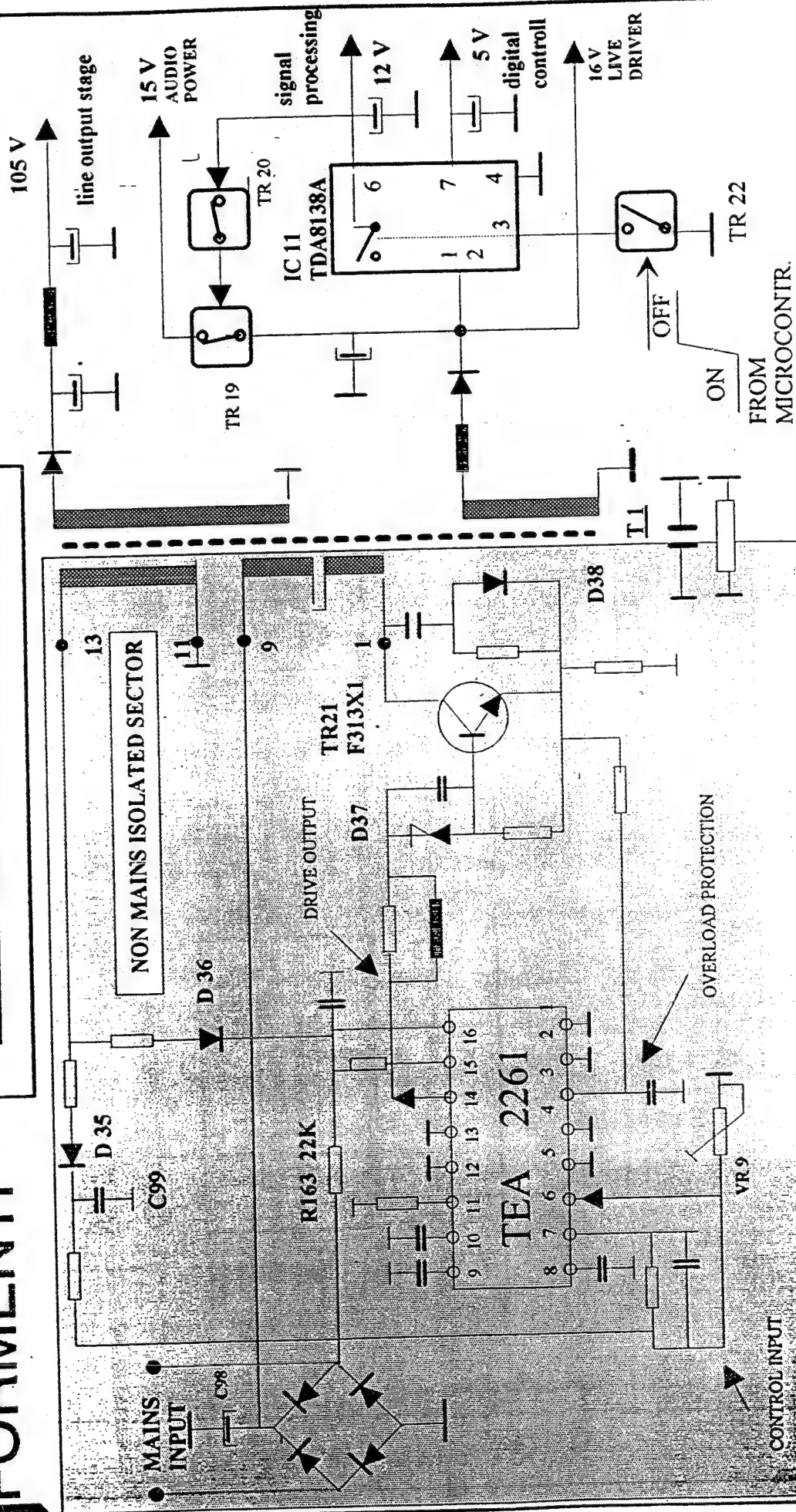
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F 14 POWER SUPPLY

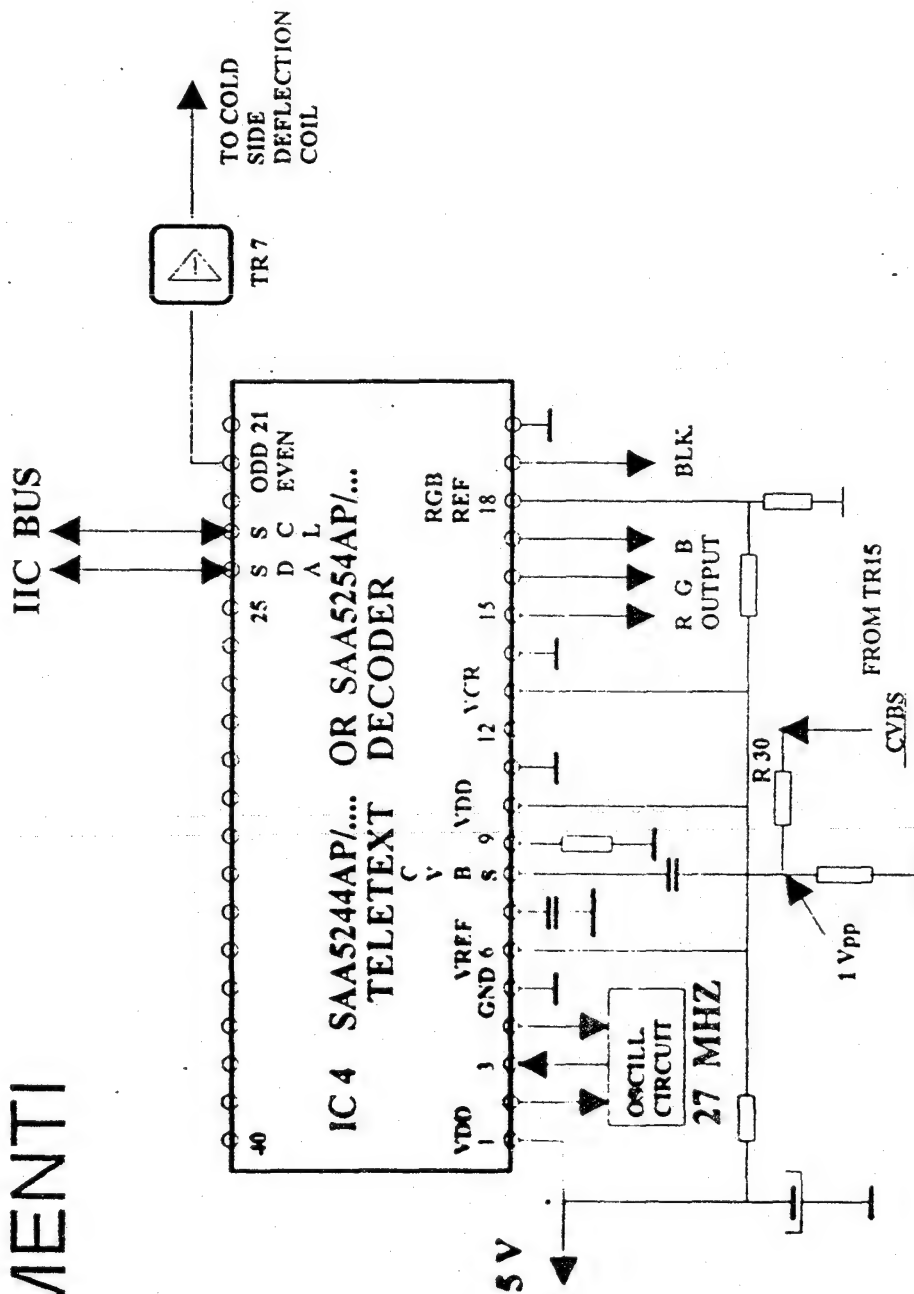


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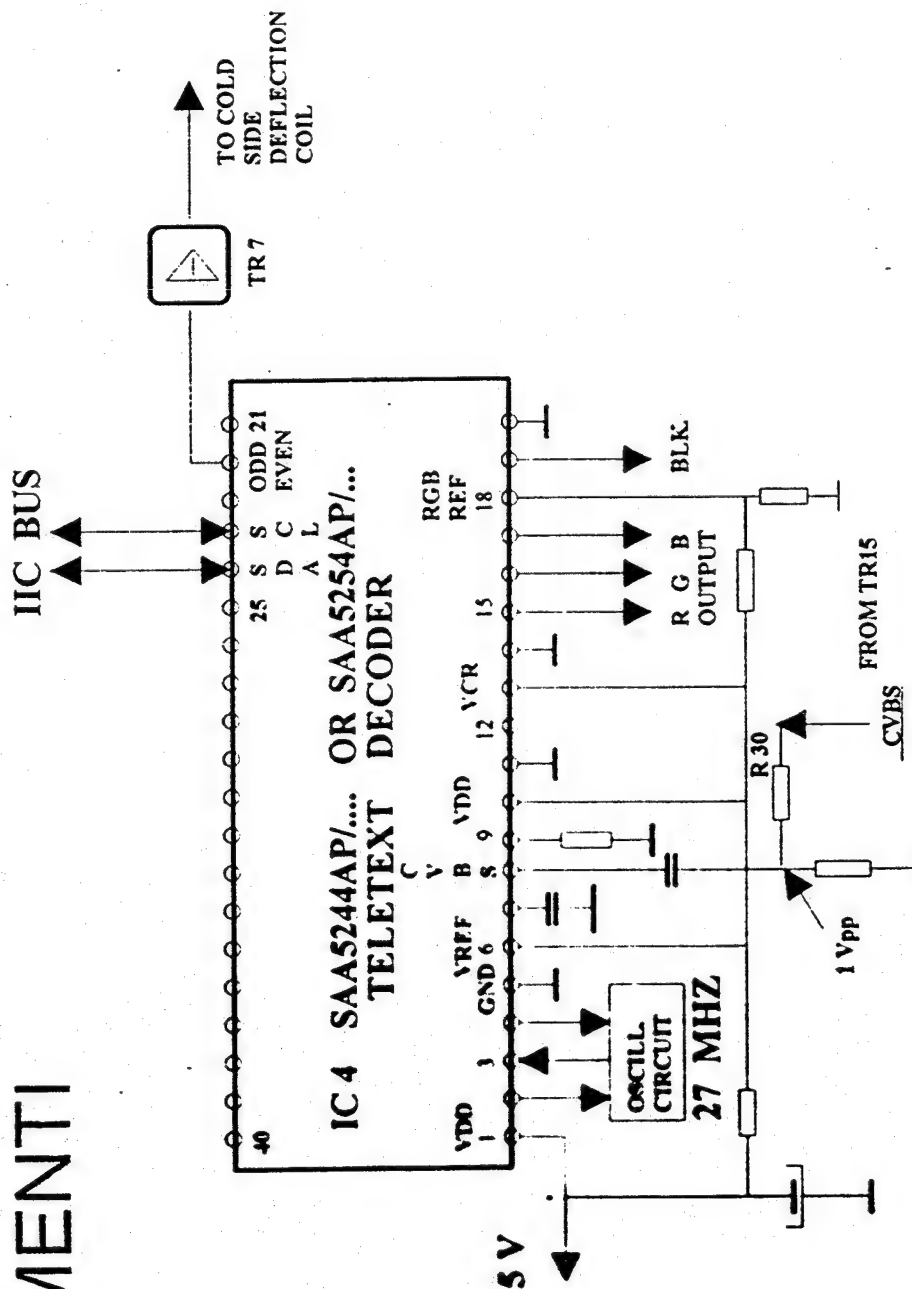
F 10 / F 12 POWER SUPPLY



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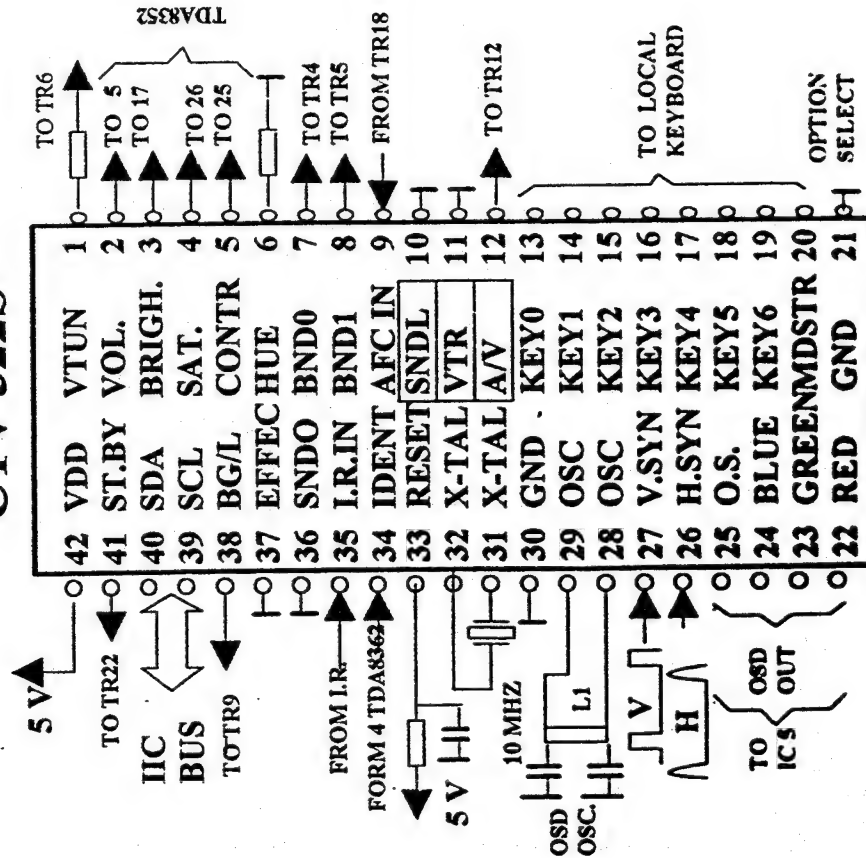
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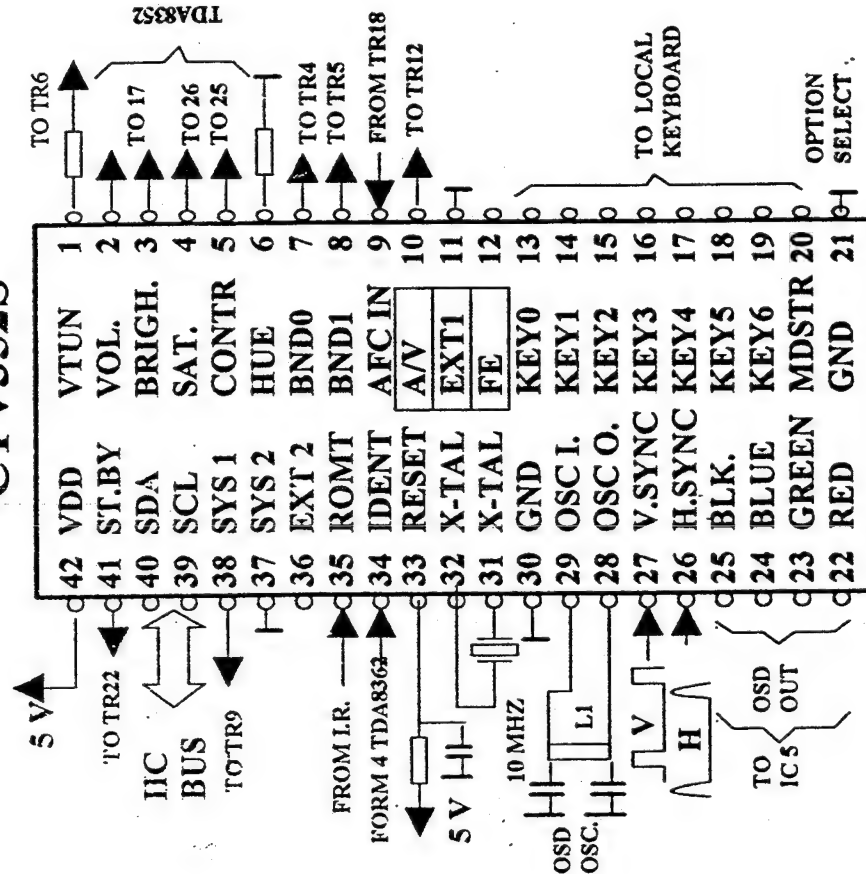
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F10, F12, & F14 MICROCONTROLLERS

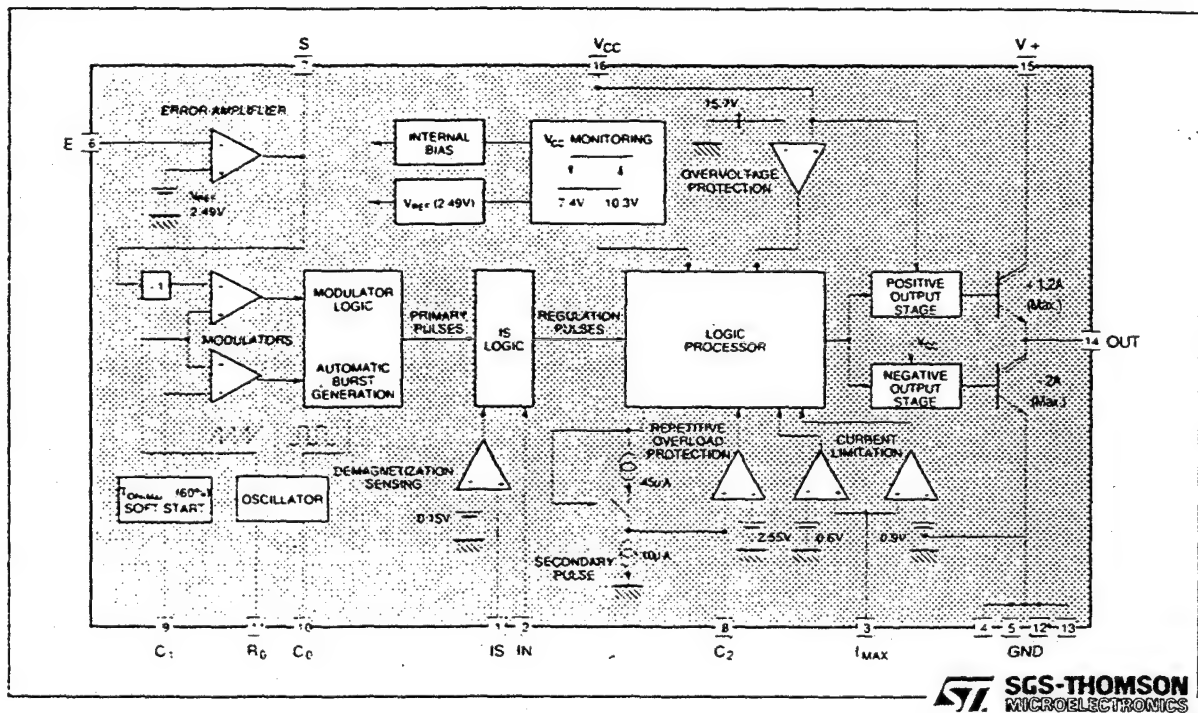
F10 & F14 CTV 322S



F12 CTV352S



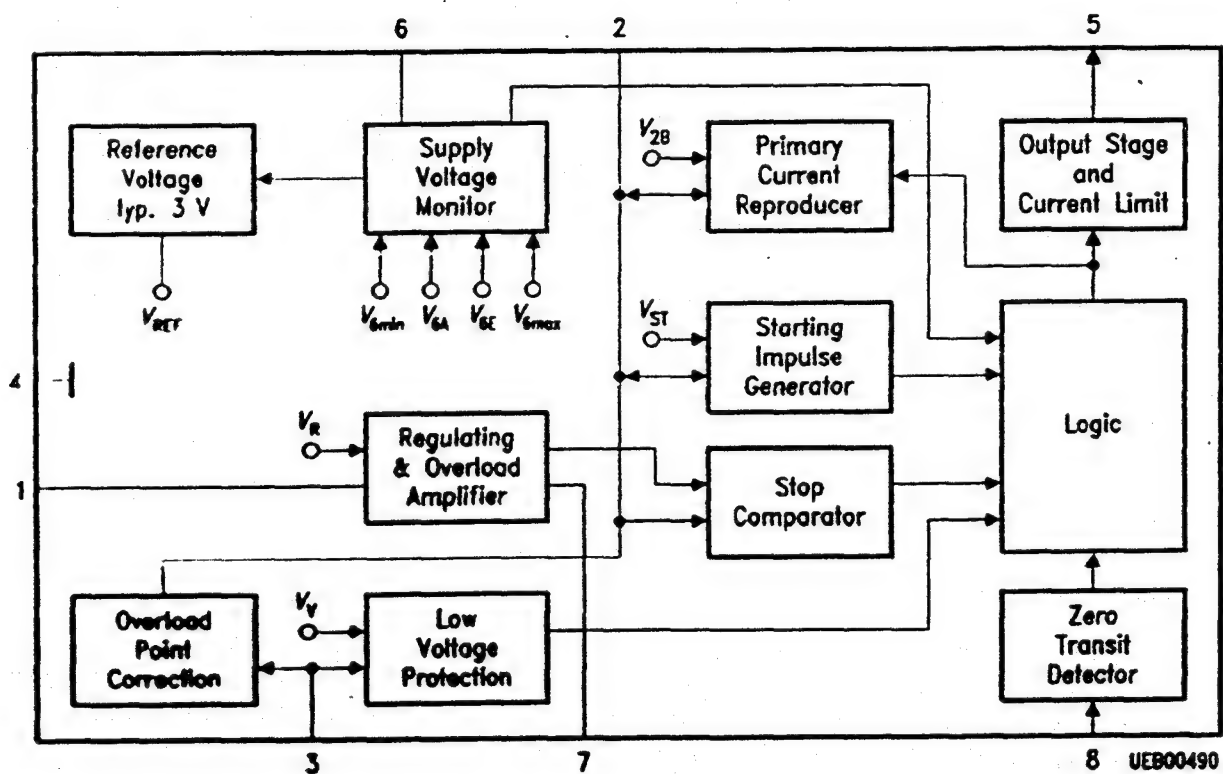
POWER SUPPLY - TEA 2261



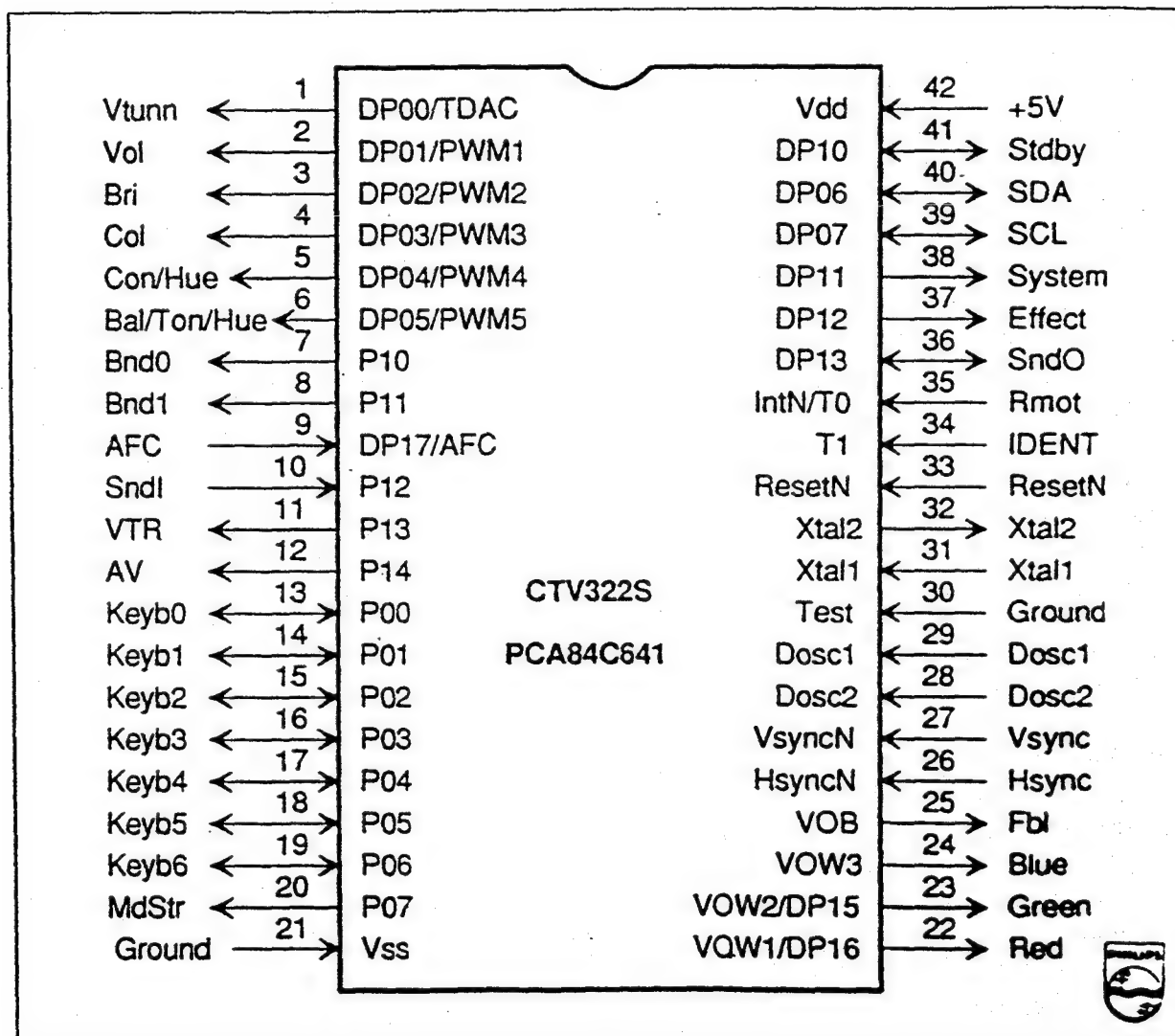
Functional description

Integrated circuit TEA 2261 is a switch-mode power controller that is particularly suited to TV use. It is able to directly drive a bipolar current with a base current of 1.2 A. . It is a controller complete with all functions for normal operation, for transient operation (ex. soft-start), and for malfunction operation (protection against overload and short-circuits).

POWER SUPPLY - TDA 4605



TUNING - PCA 84C641/524 CTV322S



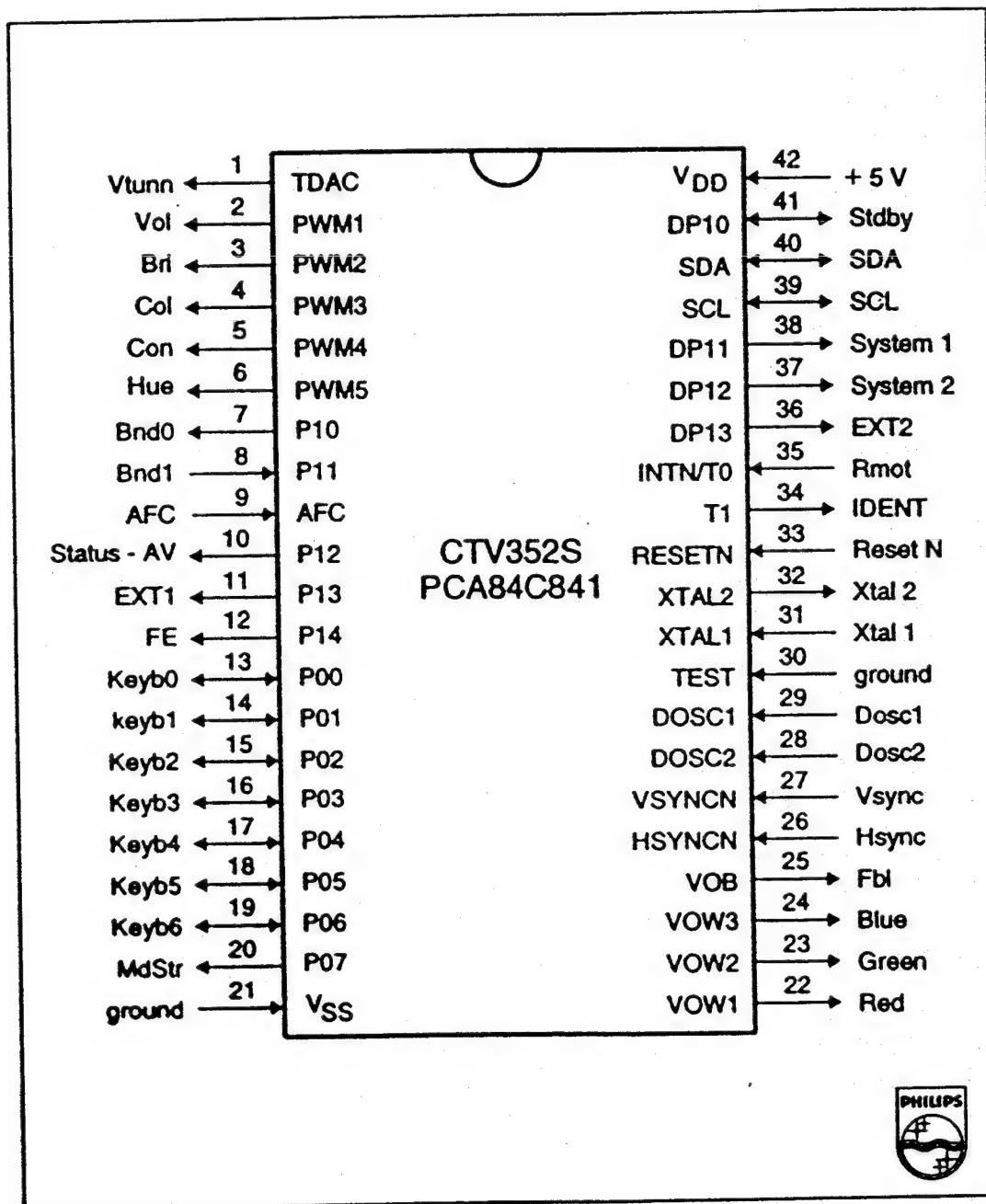
PCA84C641/524 CTV322S pinout description

- 1- tuning voltage output
- 2- volume output
- 3- brightness output
- 4- saturation output
- 5- contrast output
- 6- hue output
- 7- bands 0 output
- 8- bands 1 output
- 9- AFC input
- 10- Dual/nonDual input
- 11- VTR output
- 12- AV audio/video output
- 13- input/output keyboard
- 14- input/output keyboard
- 15- input/output keyboard
- 16- input/output keyboard
- 17- input/output keyboard
- 18- input/output keyboard
- 19- input/output keyboard
- 20- strobe output
- 21- ground
- 22- OSD red output
- 23- OSD green output
- 24- OSD blue output
- 25- OSD fast blanking
- 26- horizontal synchro input
- 27- vertical synchro input
- 28- OSD LC oscillator
- 29- OSD LC oscillator
- 30- ground (test)
- 31- xtal 10 MHz oscillator input
- 32- oscillator output
- 33- reset
- 34- identification input
- 35- IR input
- 36- mono/stereo or A/B language
- 37- sound effects output
- 38- system output
- 39- SCL i2cbus
- 40- SDA i2cbus
- 41- stand-by
- 42- power supply

Functional description

CTV322S tuning is a control system for television based on microcontroller PCA84C641/524. It is a voltage synthesis system with OSD (On-screen-display), sound and colour are controlled by 5 digital/analog converters.

TUNING - PCA 84C841 CTV352S



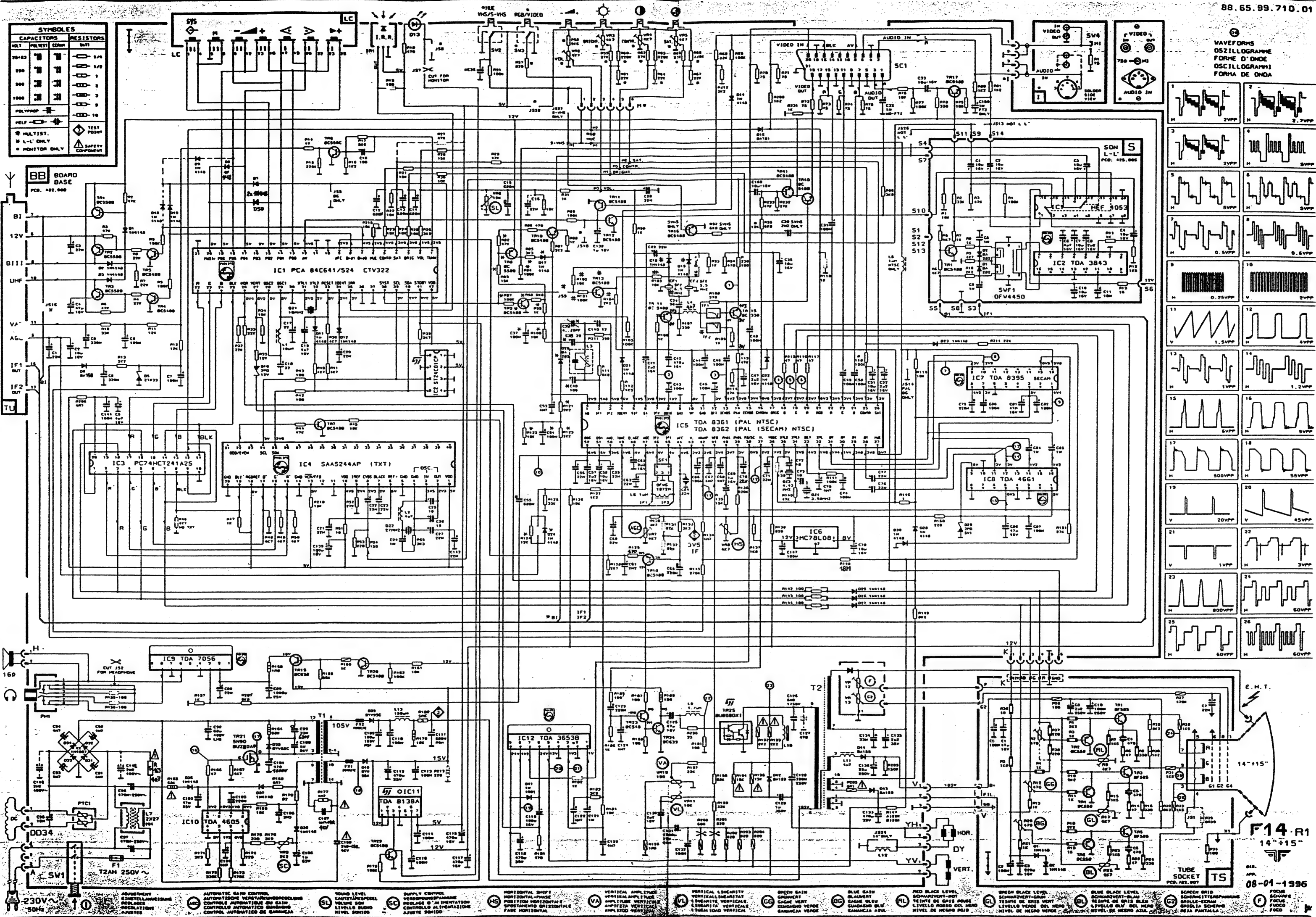
PCA84C841 CTV352S pinout description

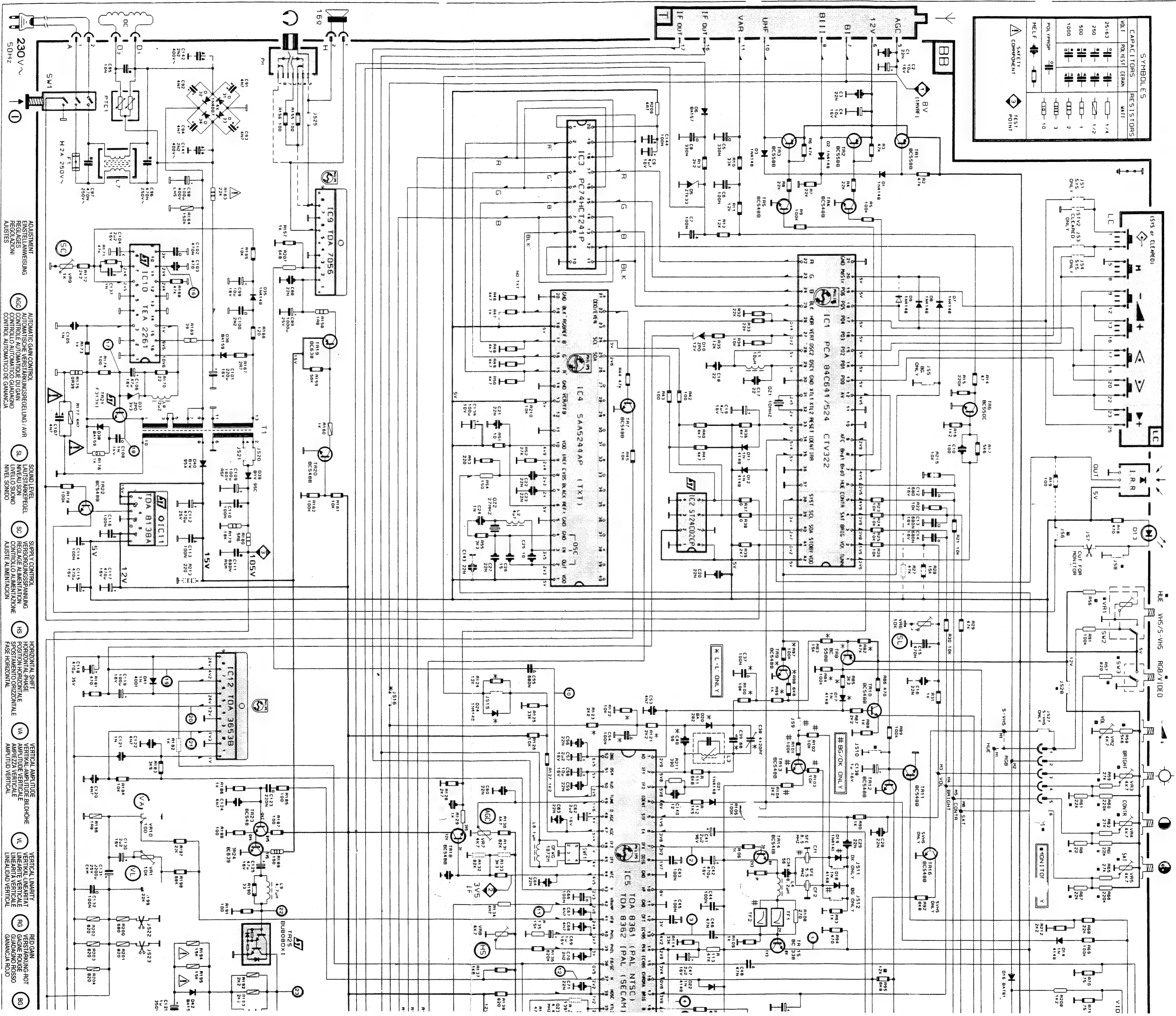
- 1 - tuning voltage output
- 2 - volume output
- 3 - brightness output
- 4 - saturation output
- 5 - contrast output
- 6 - hue output
- 7 - band-switch 0 output
- 8 - band-switch 1 output
- 9 - AFC input
- 10 - AV status input
- 11 - external source select output
- 12 - Av audio/video output
- 13 - input/output keyboard
- 14 - input/output keyboard
- 15 - input/output keyboard
- 16 - input/output keyboard
- 17 - input/output keyboard
- 18 - input/output keyboard
- 19 - input/output keyboard
- 20 - strobe output
- 21 - ground
- 22 - OSD red output
- 23 - OSD green output
- 24 - OSD blue output
- 25 - OSD fast blanking
- 26 - horizontal synchro input
- 27 - vertical synchro input
- 28 - OSD LC oscillator
- 29 - OSD LC oscillator
- 30 - ground (test)
- 31 - xtal 10 MHz oscillator input
- 32 - oscillator output
- 33 - reset
- 34 - identification input
- 35 - IR input
- 36 - external source select output
- 37 - system output
- 38 - system output
- 39 - SCL i2cbus
- 40 - SDA i2cbus
- 41 - stand-by
- 42 - power supply

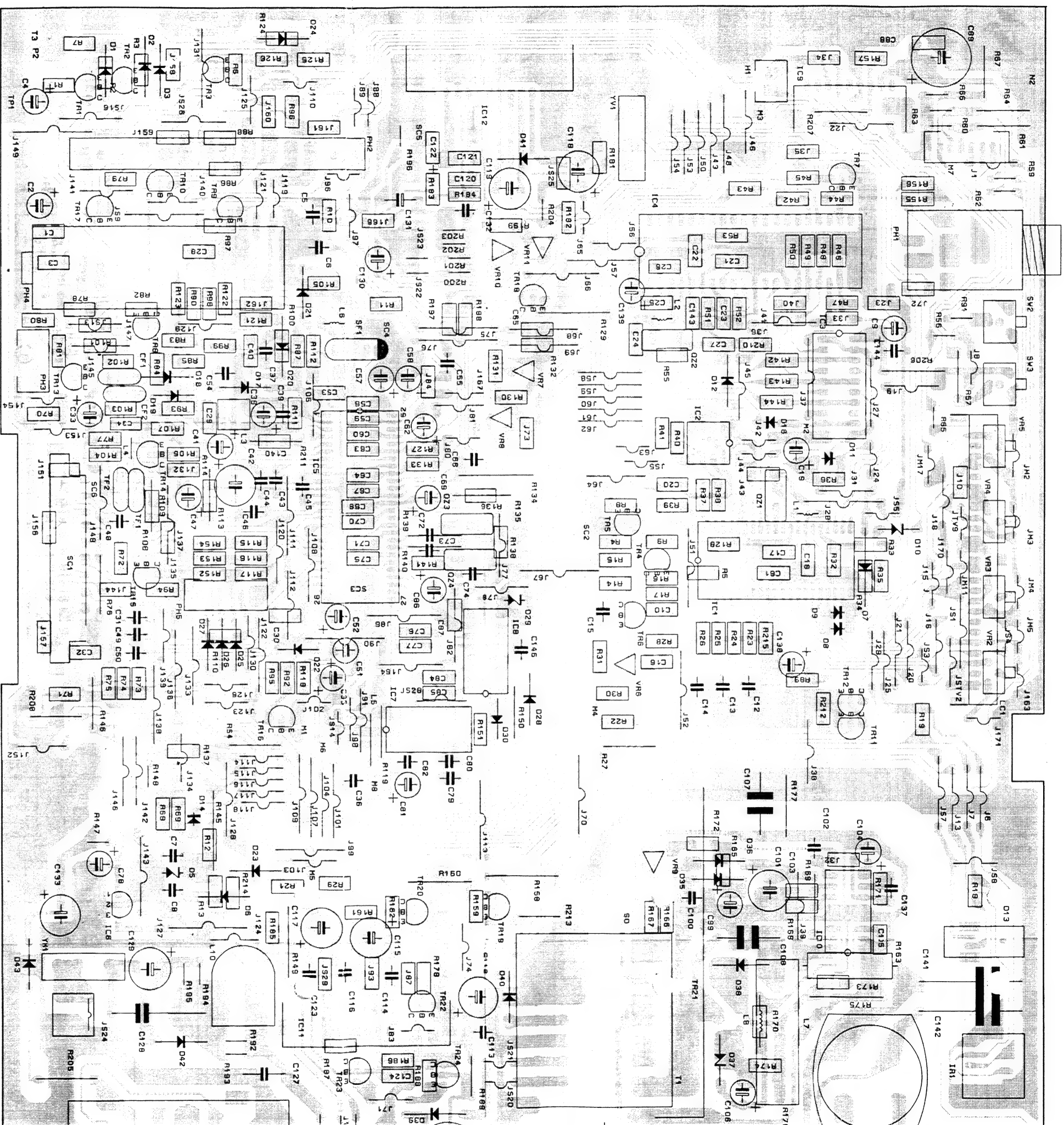
Functional description

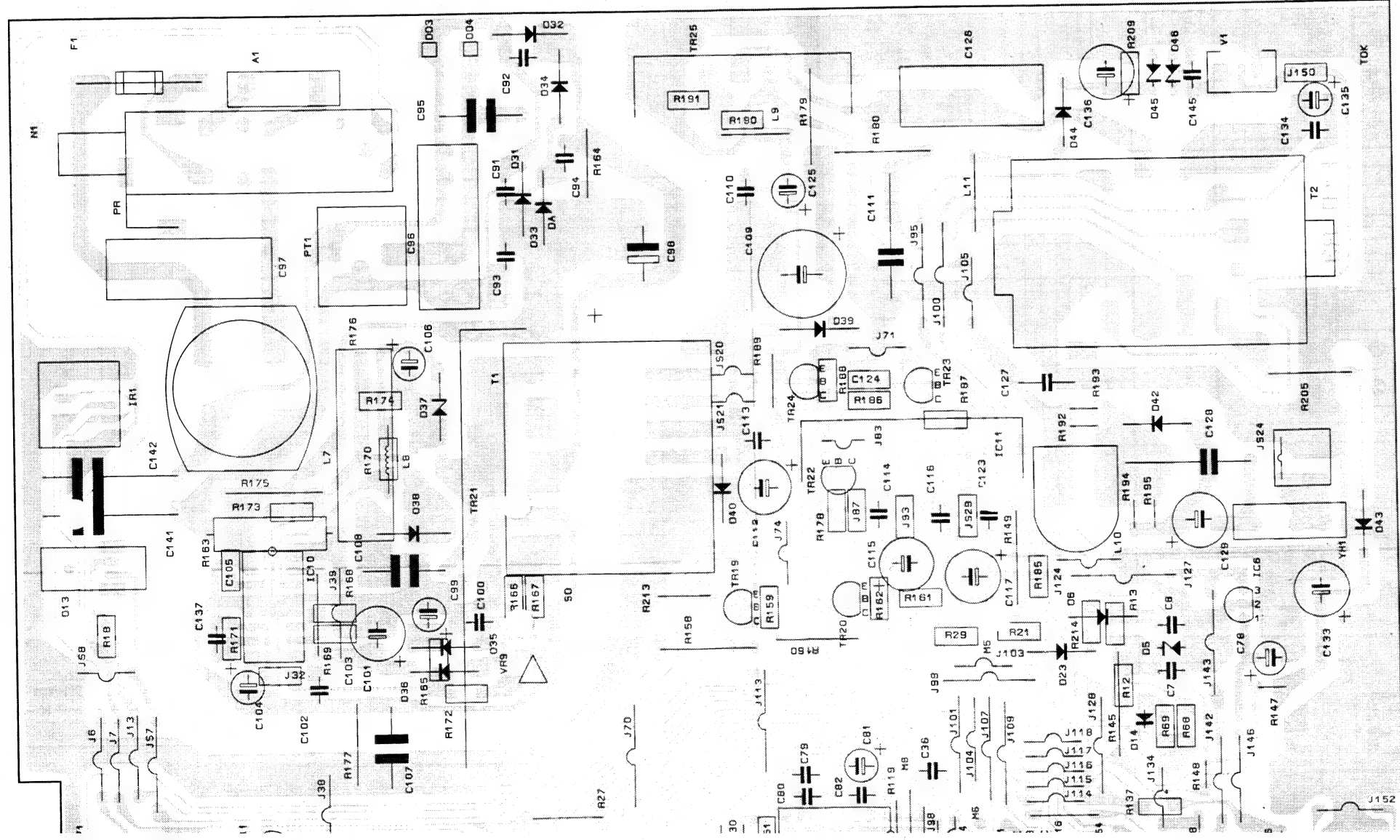
CTV352S tuning is a control system for television based on microcontroller PCA84C841.

It is a voltage synthesis system with OSD (On-screen-display), sound and colour are controlled by 5 digital/analog converters.

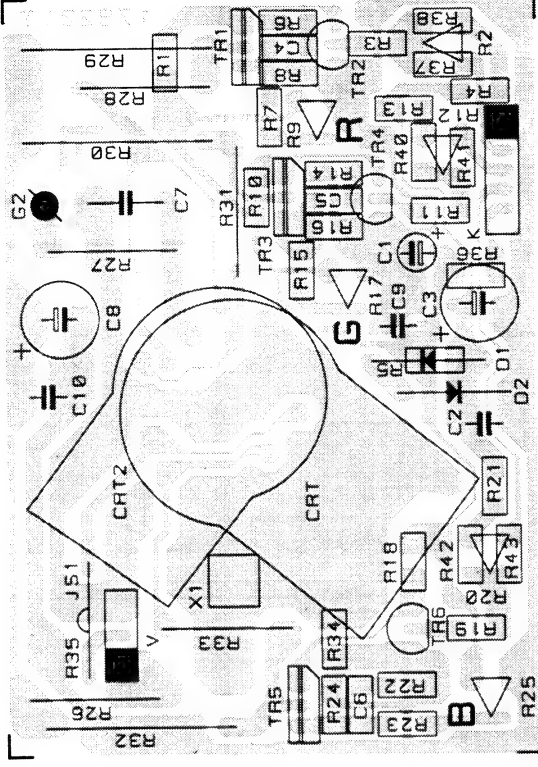




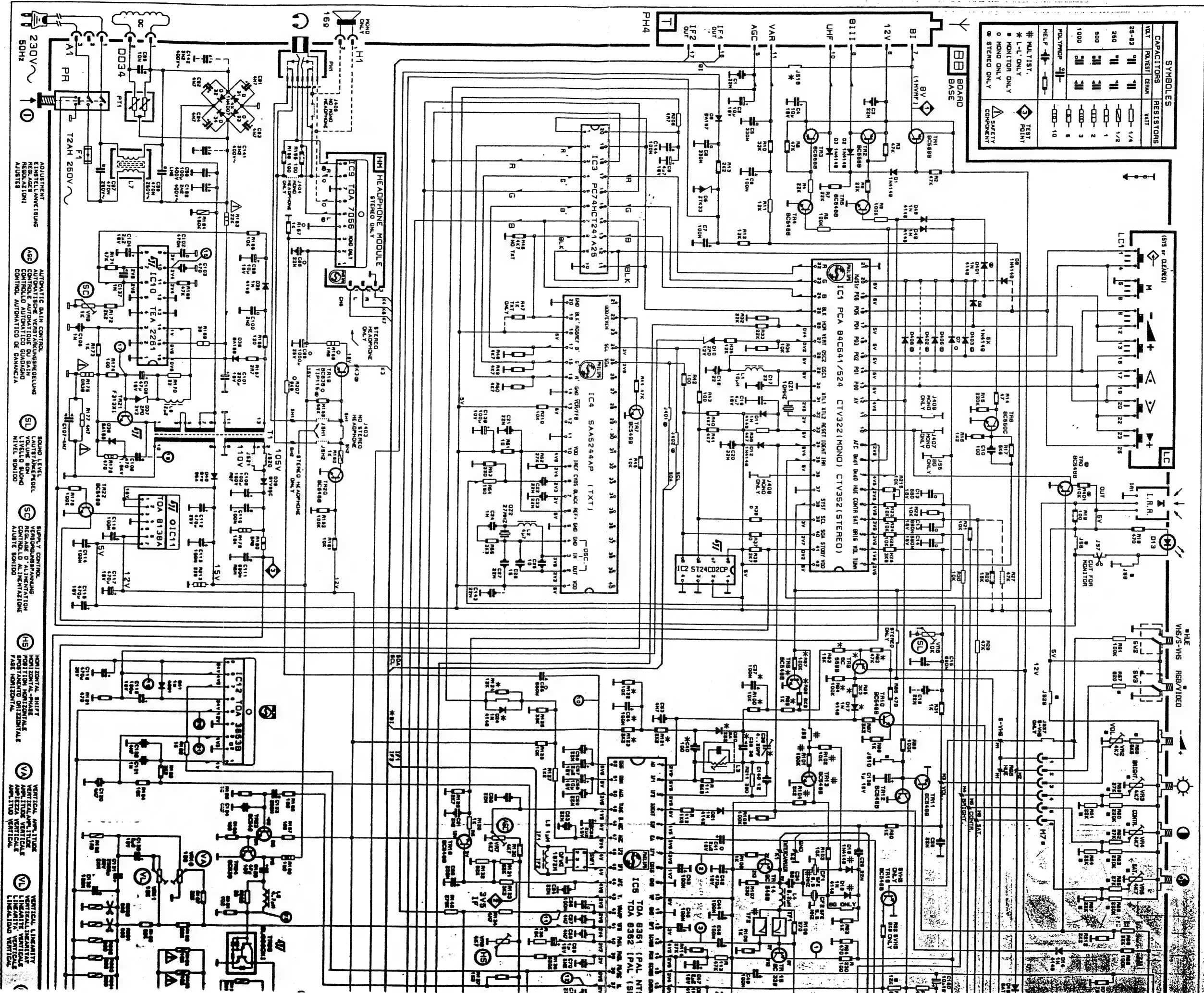


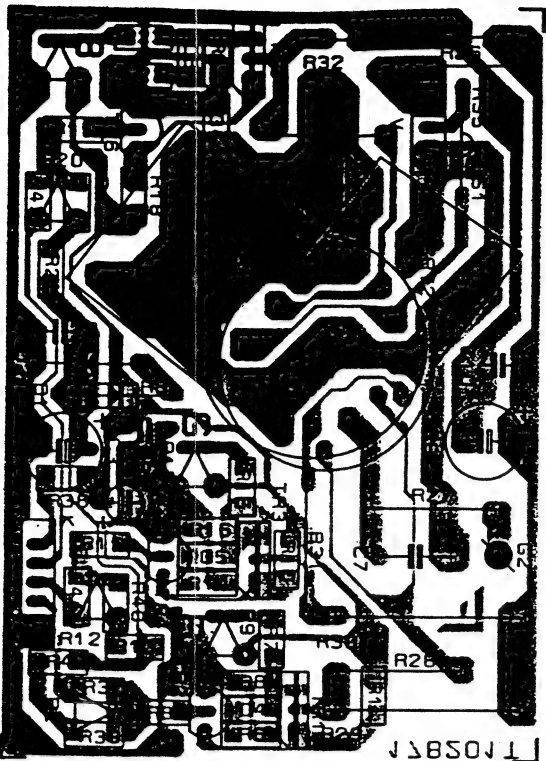
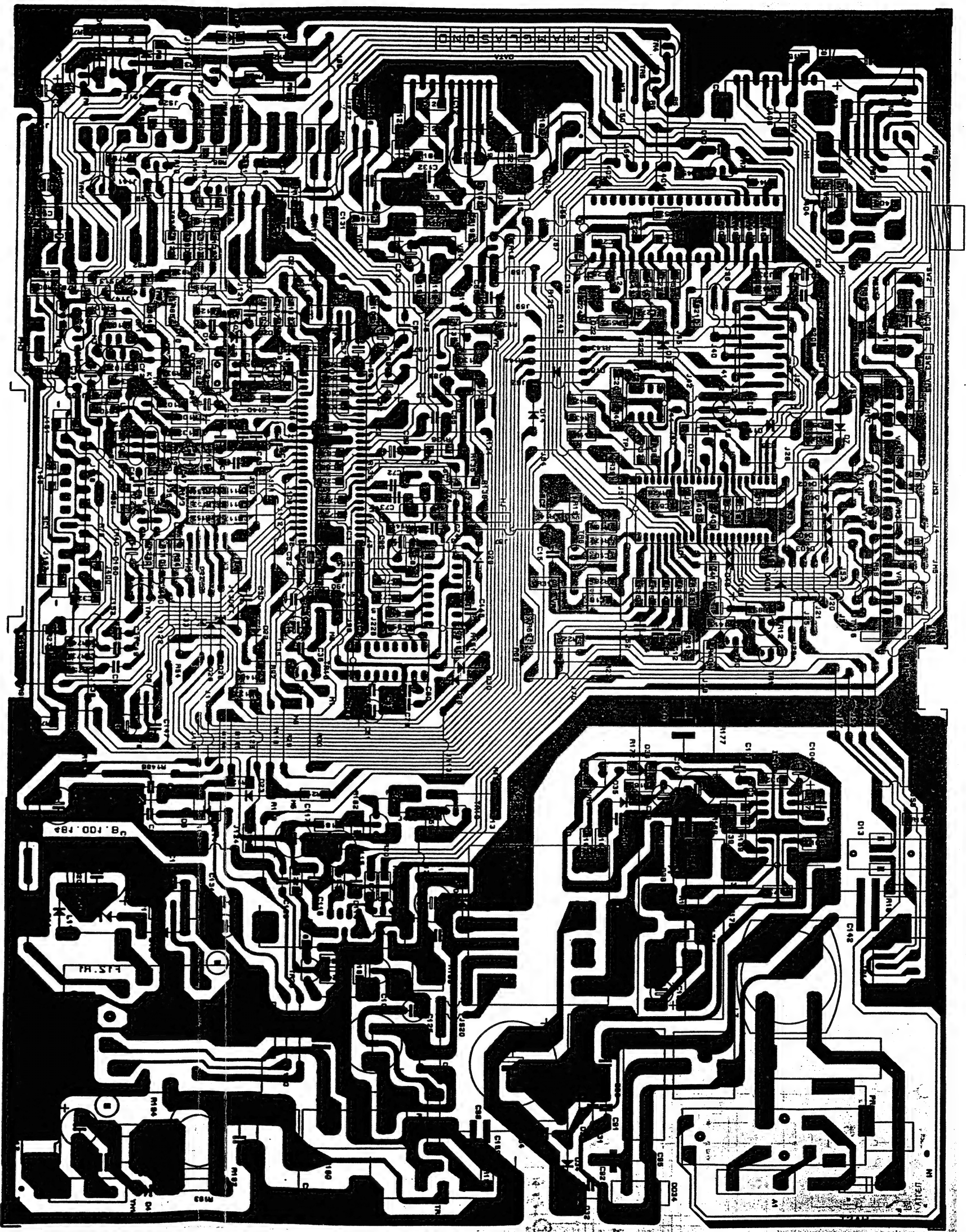


UITO IMPRESO CHASIS

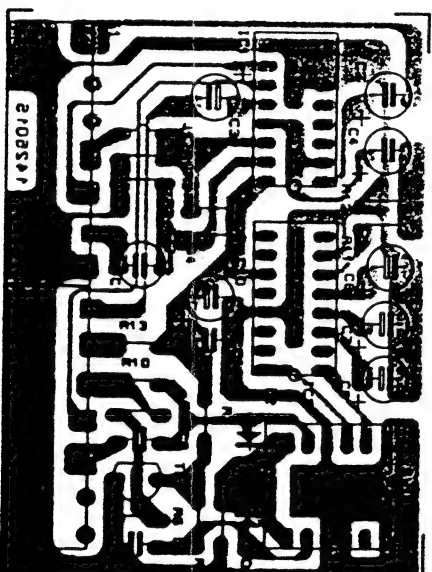


TUBE SOCKET
BILDROEHRENSOCKEL
SUPPORT TRC
ZOCOLO CINESCOPIO
CIRCUITO IMPRESO ZOCALO

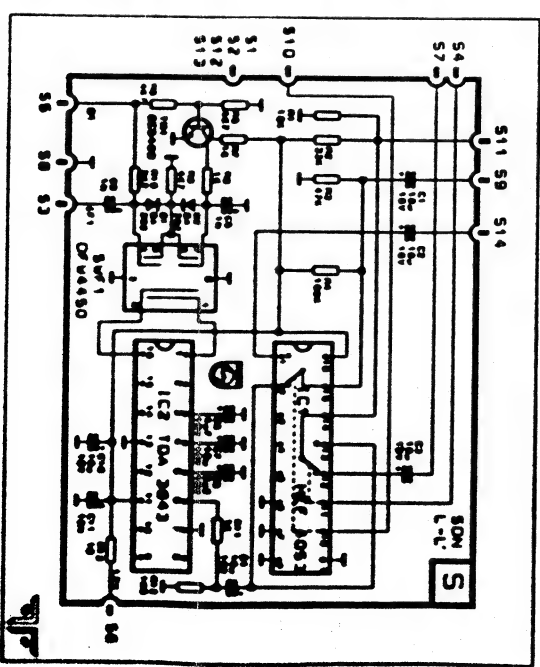


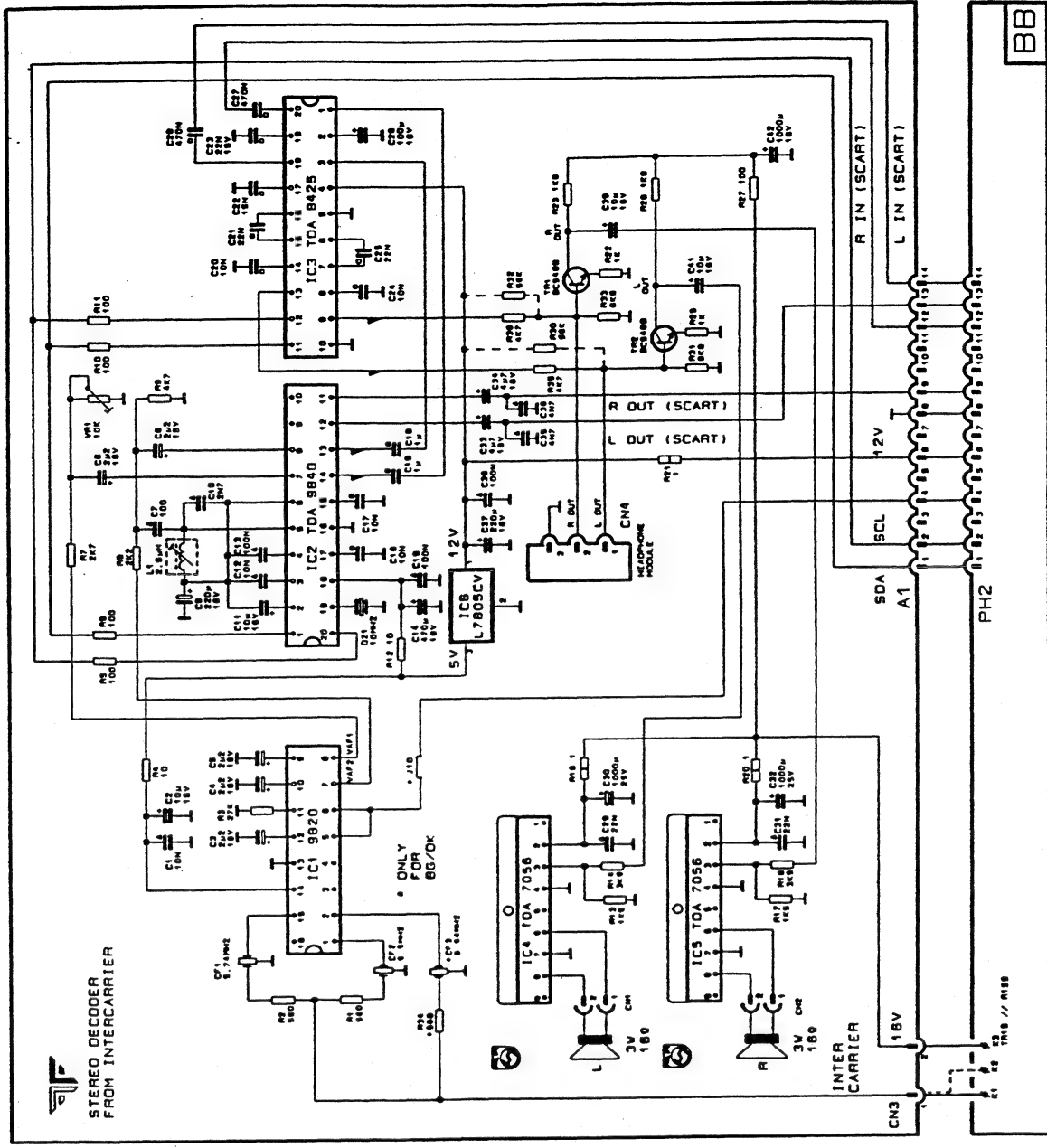
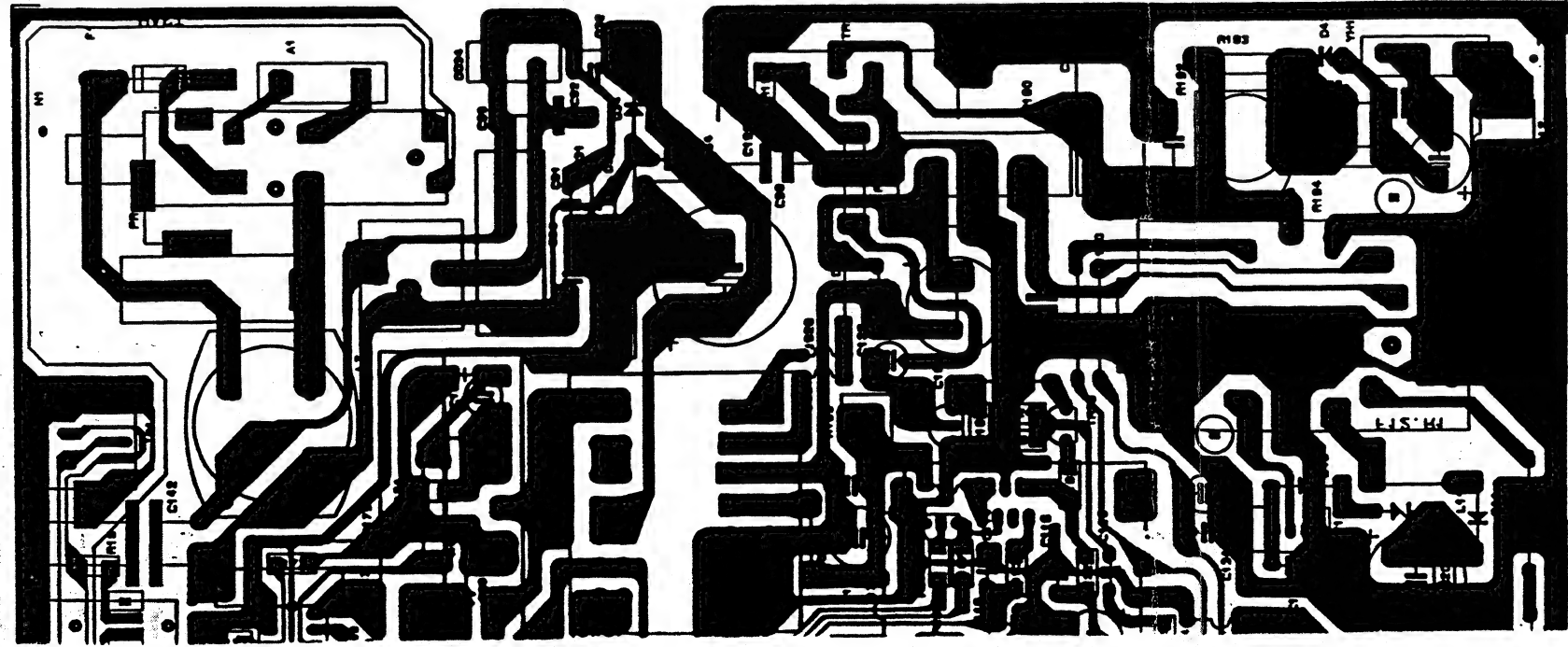


TUBE SOCKET
BILDROEHRENSOCKEL
SUPPORT TRC
ZOCOLO CINESCOPIO
CIRCUITO IMPRESO ZOCALO



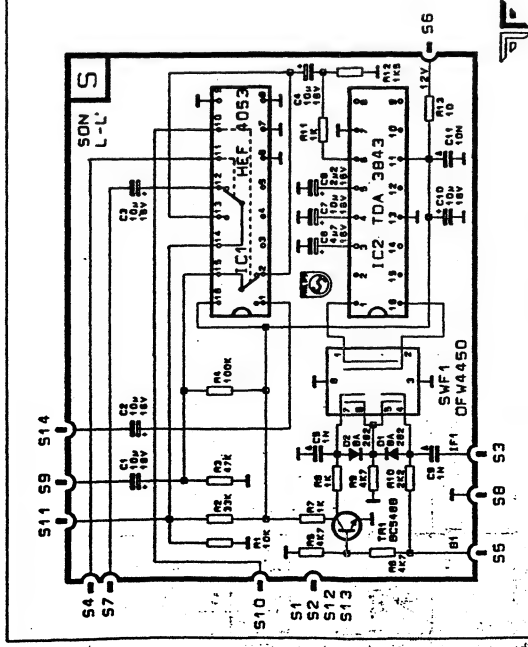
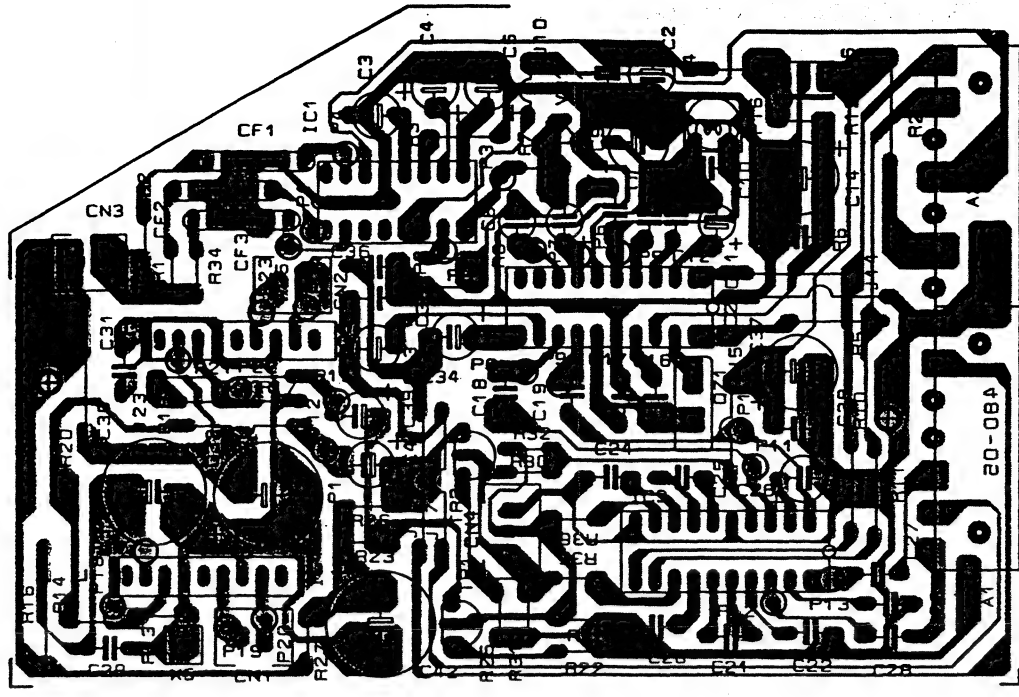
AUDIO/L
AUDIO/L
SON/L
AUDIO/L





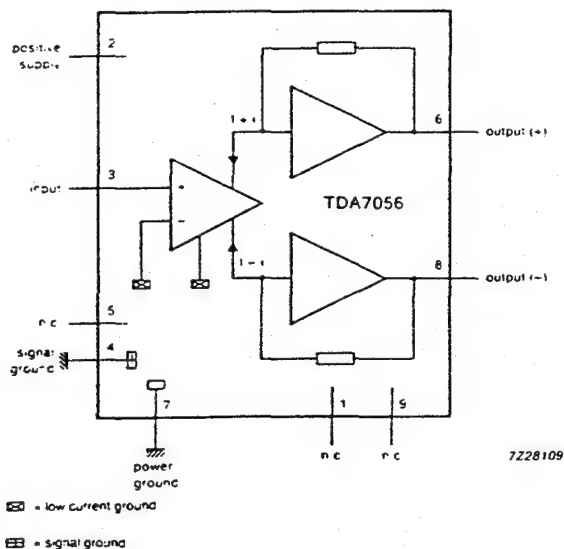
STEREO DECODER
STEREO TON
MODULE SON STEREO
AUDIO STEREO
SONIDO STEREO

BOARD BASE
GRUNDCHASSIS
PLATINE MERE
TELAIO BASE
CIRCUITO IMPRESO CHASSIS



HEADPHONES AMPLIFIER
KOPFHÖRER VERSTÄRKER
AMPLIFICATORE CUFFIA
AMPLIFICADOR AURICULARES

AUDIO - TDA 7056 - FOR MONO VERSION



TDA 7056 pinout description

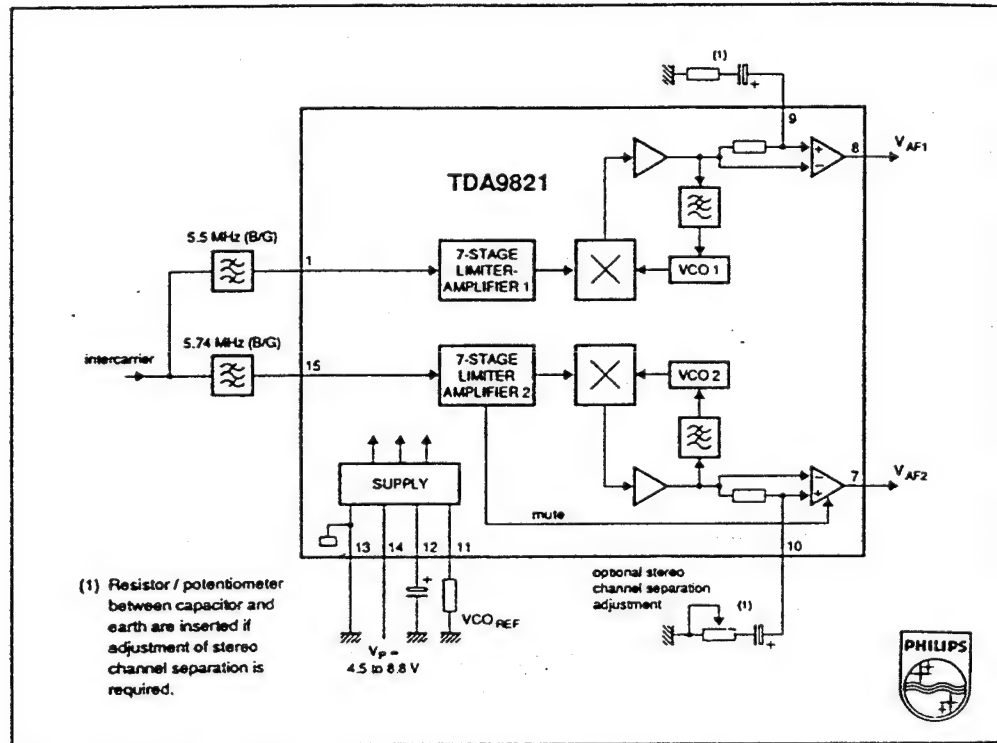
- 1 - n.c.
- 2 - power supply
- 3 - input (+)
- 4 - signal ground
- 5 - n.c.
- 6 - output (+)
- 7 - power ground
- 8 - output (+)
- 9 - n.c.

Functional description

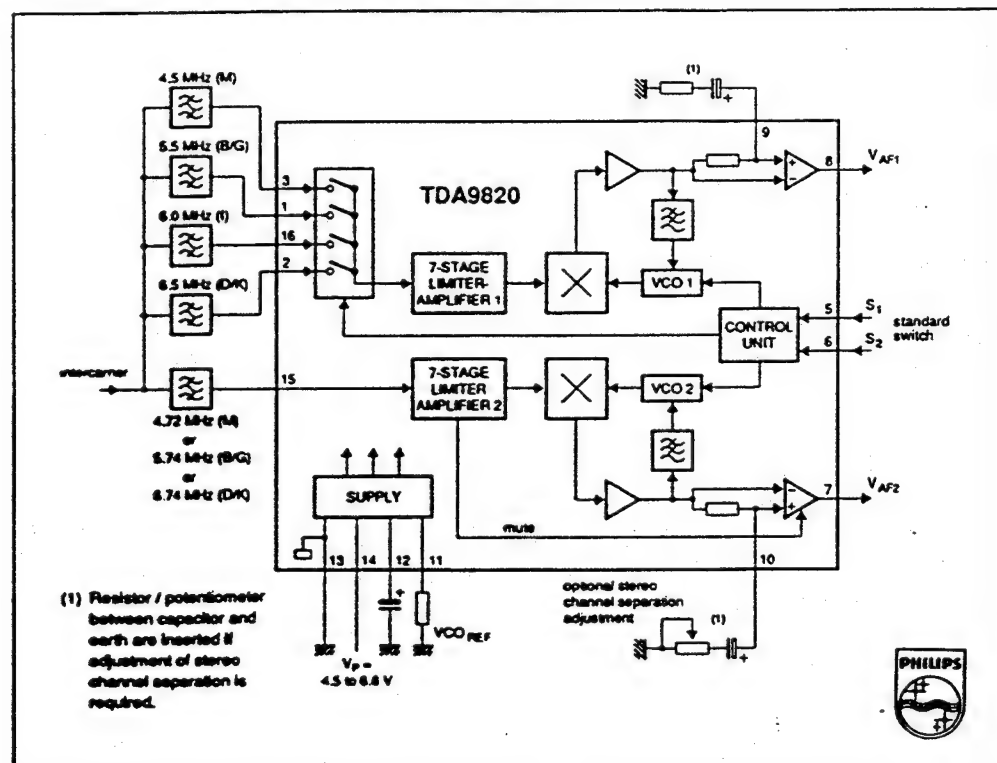
TDA 7056 is a monophonic output amplifier. It requires no external component and uses BTL (Bridge-Tied-Load) outputs. For equal power-supply voltages, it has more power than that of traditional components. It drives 16 Ohm speakers. Gain is set internally at 40 dB.

STEREO DECODER

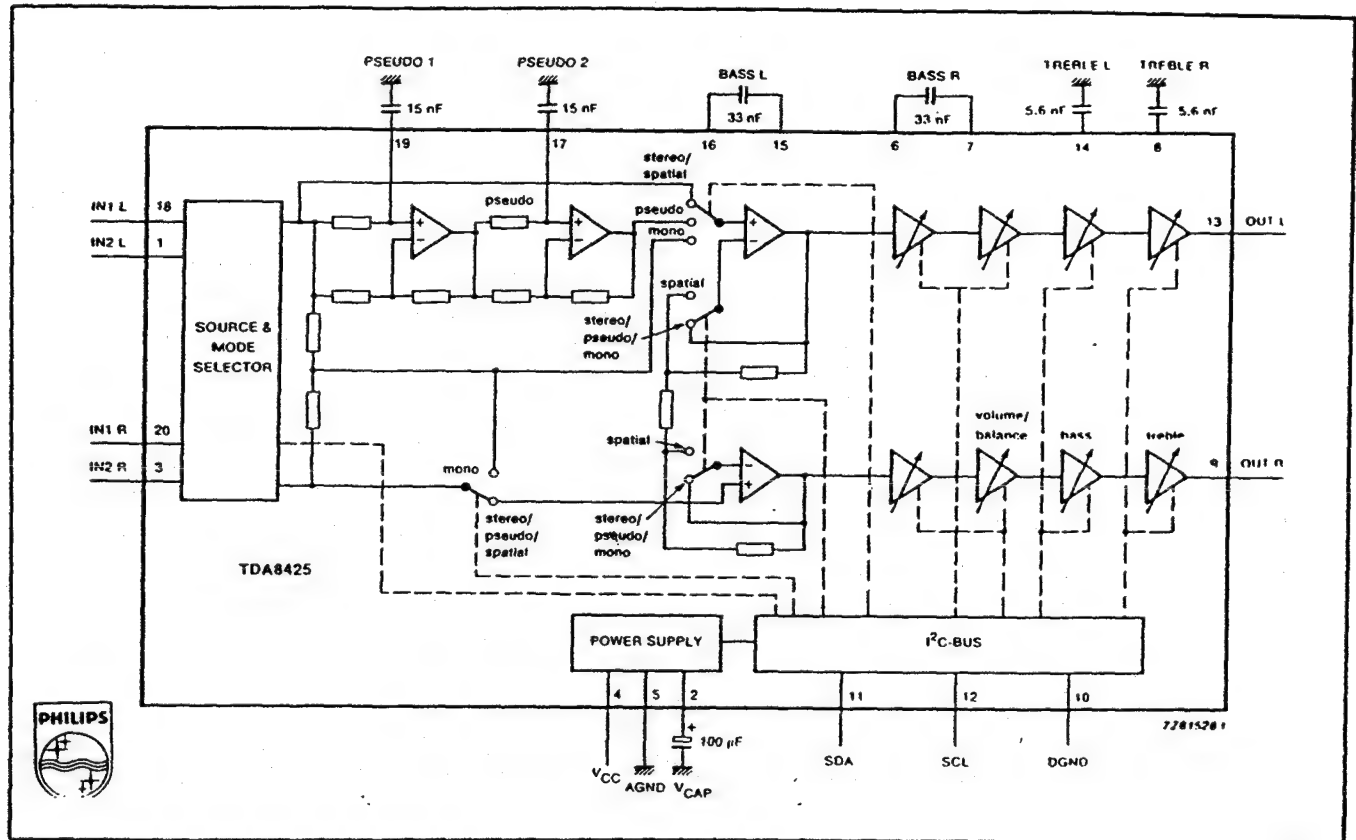
TDA 9821 : Dual channel TV FM intercarrier sound demodulator.



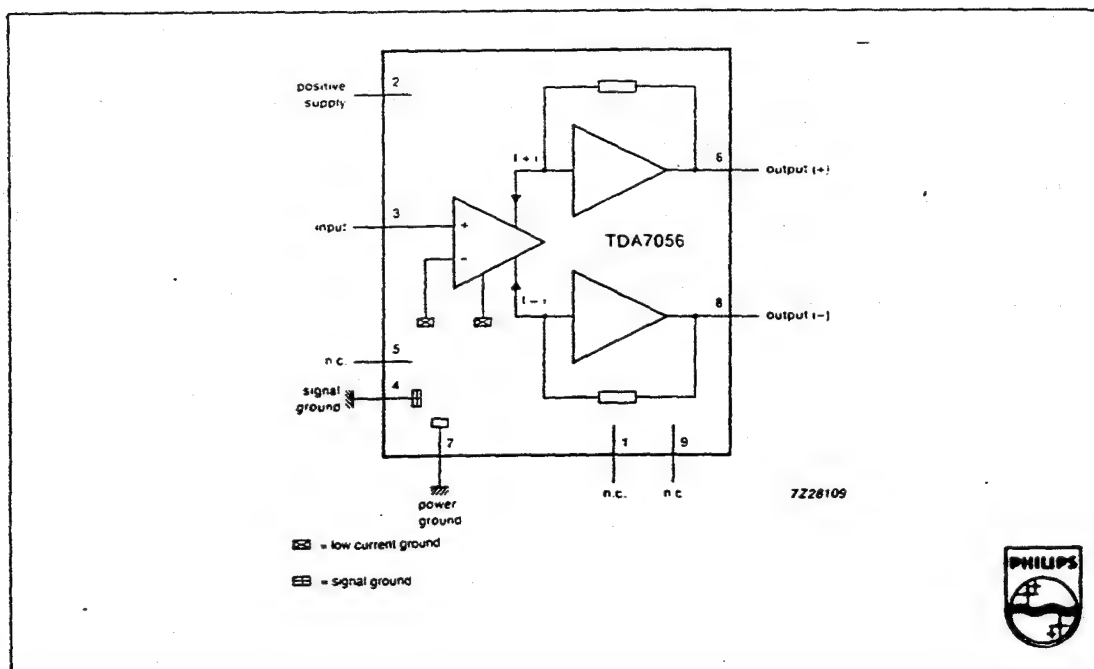
TDA 9820 : Dual channel TV FM intercarrier sound demodulator.



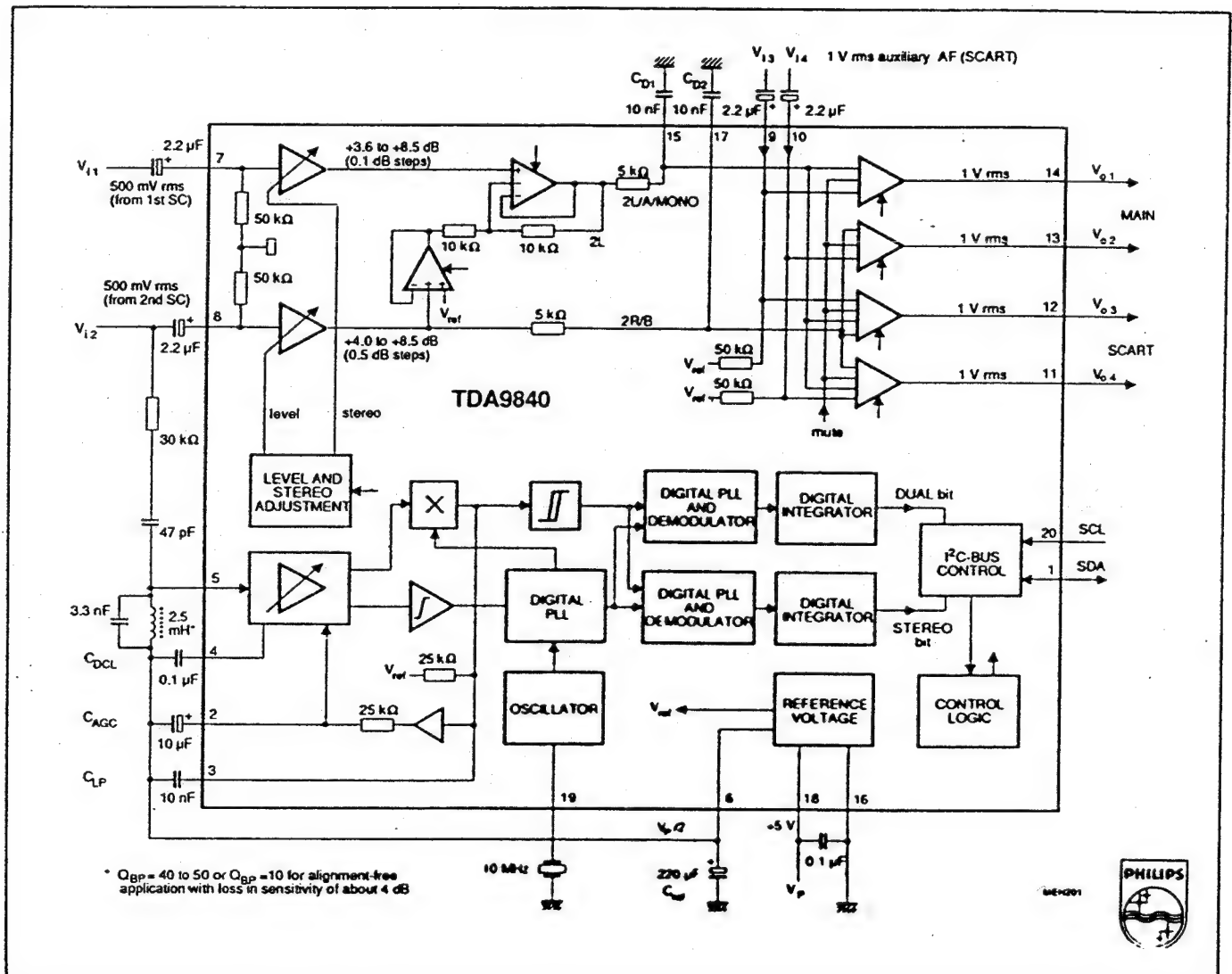
TDA 8425 : HI-FI Stereo audio processor; i2c-bus



TDA 7056 : 3 Watt mono BTL audio output amplifier.

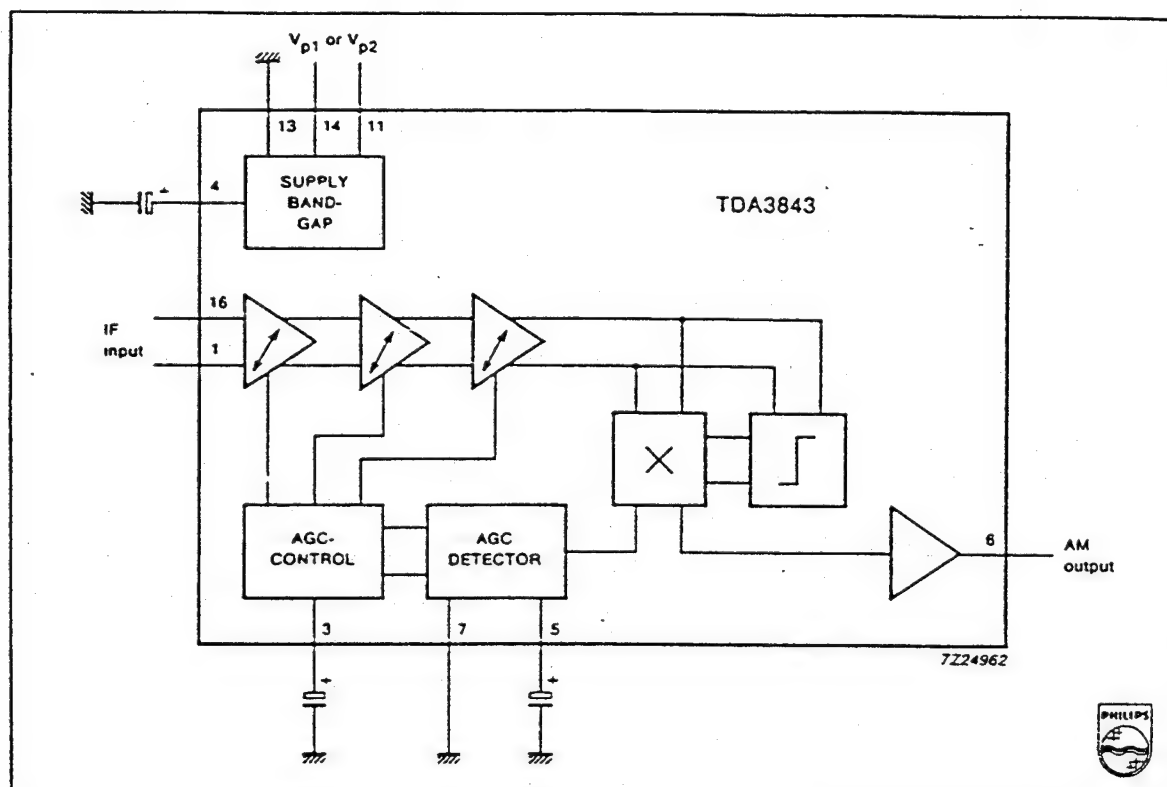


TDA 9840 : Stereo/dual sound processor with digital identification.



* $Q_{BP} = 40$ to 50 or $Q_{BP} = 10$ for alignment-free application with loss in sensitivity of about 4 dB

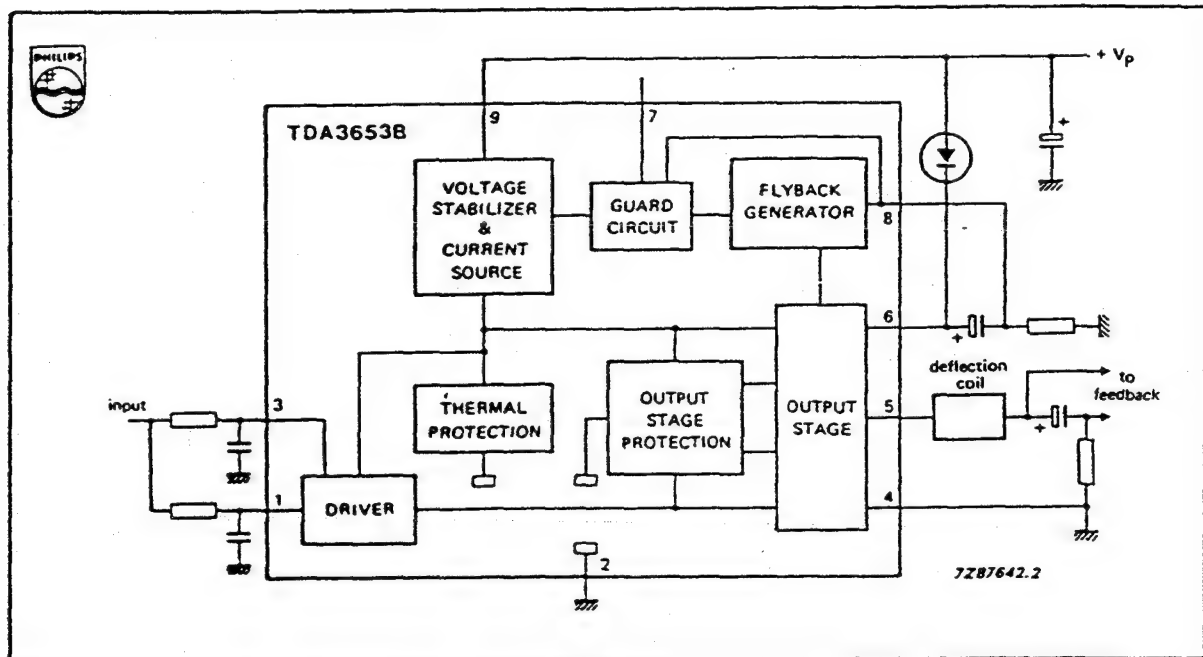
L - L' STANDARD AM AUDIO - TDA 3843



Functional description

TDA 3843 handles AM sound demodulation for standard L and L'.

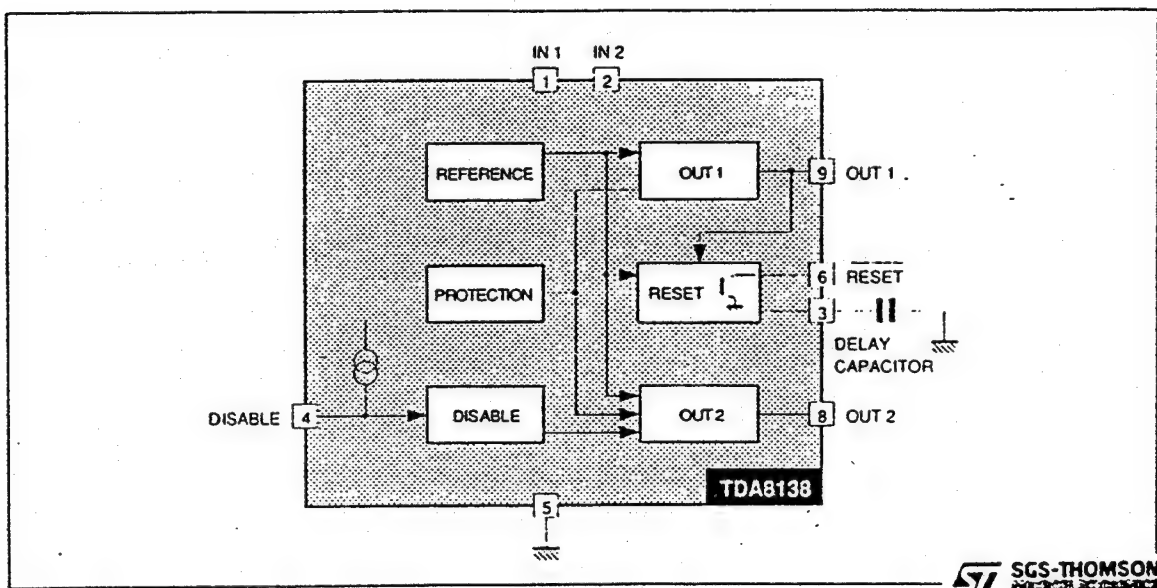
VERTICAL DEFLECTION - TDA 3653B



Functional description

TDA 3653B is a vertical deflection output circuit that drives a vertical deflection system with currents up to about 1.5 a. (usually 90°).

VOLTAGE REGULATOR - TDA 8138

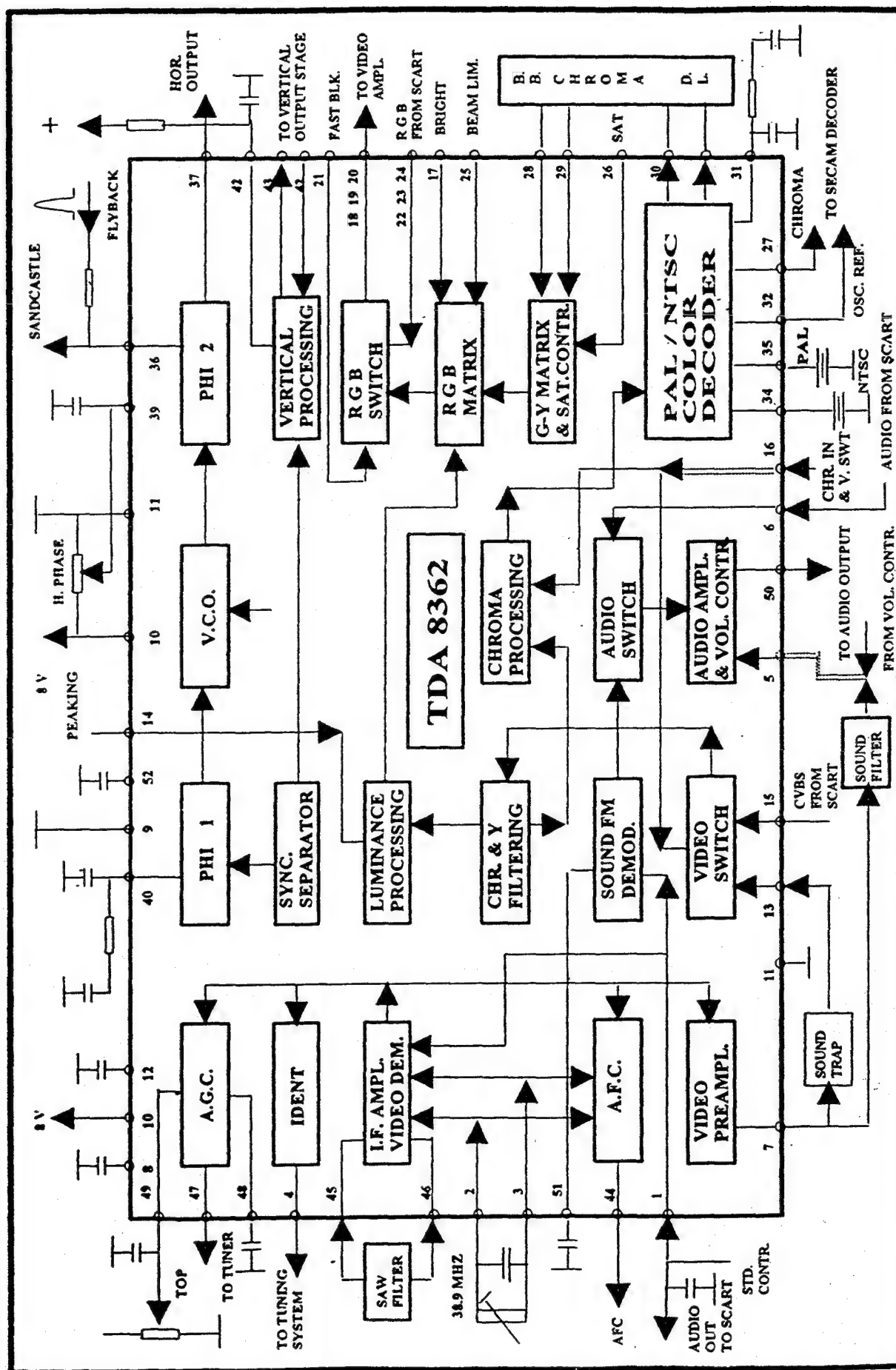


SGS-THOMSON
MICROELECTRONICS

Functional description

TDA 8138 is a dual positive voltage regulator designed to provide an voltage of 5.1 V. and 12 V. for current up to 1 A. Output 2 may be disabled by a TTL signal. TDA 8138 has thermal protection against short circuits.

MONOCHIP - TDA 8362



MONOCHIP - PIN DESCRIPTION FOR TDA 8362

- 1 - de-emphasise + positive and negative modulation
- 2 - demodulator input
- 3 - demodulator input
- 4 - identification output
- 5 - IF sound input+ volume control
- 6 - external sound input
- 7 - IF video output
- 8 - digital section decoup.
- 9 - ground
- 10 - power supply
- 11 - ground
- 12 - tuning decoup.
- 13 - video input
- 14 - peaking
- 15 - external video input
- 16 - A/V input + chroma input
- 17 - brightness
- 18 - Blue output
- 19 - Green output
- 20 - Red output
- 21 - fast blanking input
- 22 - external Red input
- 23 - external Green output
- 24 - external Blue output
- 25 - contrast
- 26 - saturation
- 27 - hue + chroma output
- 28 - B-Y input
- 29 - R-Y input
- 30 - R-Y output
- 31 - B-Y output
- 32 - 4.43 Mhz ref. output
- 33 - phase detector
- 34 - 3.58 Mhz input
- 35 - 4.43 Mhz input
- 36 - Horizontal oscillator start
- 37 - horizontal drive output
- 38 - sandcastle/flyback output/input
- 39 - if filter 2
- 40 - if filter 1
- 41 - vertical feedback input
- 42 - vertical ramp generator
- 43 - vertical drive output
- 44 - AFC output
- 45 - IF input
- 46 - IF input
- 47 - AGC output
- 48 - AGC decoup.
- 49 - AGC regulation
- 50 - audio output
- 51 - sound demod decoup
- 52 - power-supply decoup.

Differences with respect to TDA 8361

- pin 1 solely audio de-emphasise
- pin 27 solely hue
- pin 32 4.43 Mhz output not connected

Functional description of monochip TDA 8361/2

-IF Amplifier

The amplifier contains three differential stages with typical 60 dB dynamic control. the demodulator's polarity is suited for both positive and negative modulation in the TDA 8362 version (multi-standard PAL, SECAM, L L'), and for only negative modulation in TDA 8361.

The AFC circuit is driven by the same reference signal as the video demodulator. The AFC output voltage varies in the range 0/-6 V. . The circuit for identifying the presence of the signal in the transmission channel works independently of the synchronisation circuit : 0 V. no identification and chroma frequency 3.58 MHz.

The AGC system controls the IF amplifier gain is such a way that the amplitude of the output video signal remains constant. The voltage of the AGC capacitor (pin 48) takes into account the IF amplification level. A second loop acts on the tuner to amplify the IF input. The amplification level is regulated externally by potentiometer VR 7.

-Sound circuit

The inter-carrier signal is amplified/limited and demodulated by a PLL (phase locked loop). The PLL circuit automatically locks onto the incoming signal. The volume controls the amplitude of the composite audio signal (pin 5) . (700 mV max).

-Horizontal and vertical synchronisation circuit

Upstream of the sync. separator there is an amplifier that raises the synchronism pulse to a fixed level. The separated synchronism pulses are forwarder to the phase and coincidence detectors. The coincidence detector is used to synchronise the line oscillator and to identify the transmission channel. The integrated circuit contains a start-up circuit for the horizontal output (pin 36). The driving pulses for the vertical are generated by a divided circuit. The components for the generation of the vertical ramp are connected to pin 42. The feedback voltage from the vertical amplification stage is connected to pin 41.

-Video filters

The integrated circuit contains a chroma trap and band-pass circuit. The filters are implemented by means of circuits with gyrators. The chroma trap is active when the chroma input pin (pin 16) is connected to ground, or directly to the power supply. If pin 16 is held at intermediate voltage, the trap does not operate and therefore S-VHS application is possible. The luminance delay line and the delay for the peaking circuit are implemented by means of circuits with gyrators.

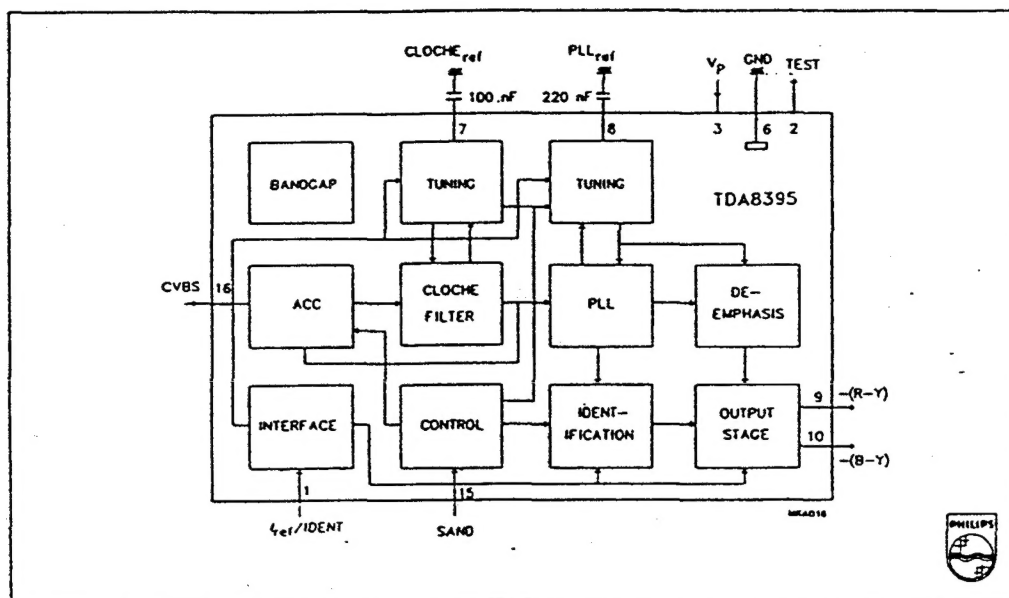
-Colour decoder

The colour decoder contains a quartz-controller oscillator, a killer circuit, and a colour difference demodulator. The 90° phase deviation is effect internally. The decoder adapts automatically to the PAL and NTSC system. For this purpose there are two pins 35 and 34. With TDA 8362, a PAL/SECAM/NTSC automatic multi-standard decoder may be built through the addition of the SECAM TDA 8395 decoder.

-RGB output circuit

The colour difference signals enter the matrices with the luminance signal to obtain the RGB signals. The integrated handles the internal signals and those coming from outside (SCART connector). Brightness and contrast act both on the internal signals and the external ones. Pin 21 of the fast blanking has a second, 4 V, threshold level. When this level is exceeded the RGB output are blocked and the OSD signals are sent directly to the output amplifier. The RGB signals have an amplitude of about 4 V. under nominal operating conditions.

SECAM DECODER - TDA 8395



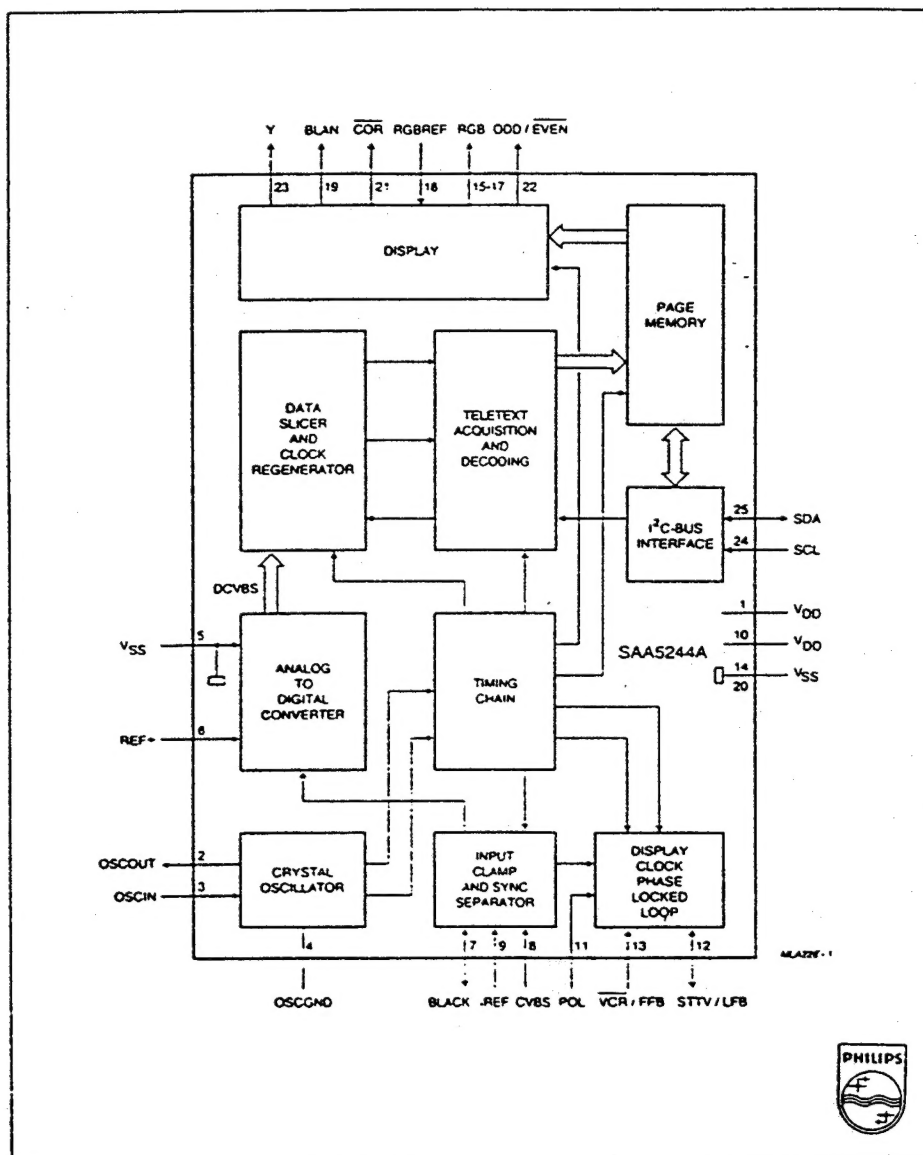
Pin description TDA 8395

- 1 - identification input
- 2 - test
- 3 - power supply
- 4 - n.c.
- 5 - n.c.
- 6 - ground
- 7 - cloche filter reference
- 8 - PLL reference
- 9 - -(R-Y) output
- 10 - -(B-Y) output
- 11 - n.c.
- 12 - n.c.
- 13 - n.c.
- 14 - n.c.
- 15 - sandcastle input
- 16 - video input

Functional description

TDA 8395 is a completely integrated SECAM decoder. The integrated circuit incorporates HF and LF filters, a demodulator, and an identification circuit. No regulation is necessary. Requirements include a stable reference frequency for calibration and a sandcastle two-level pulse for the blanking and burst gating functions.

TELETEXT - SAA 5244A

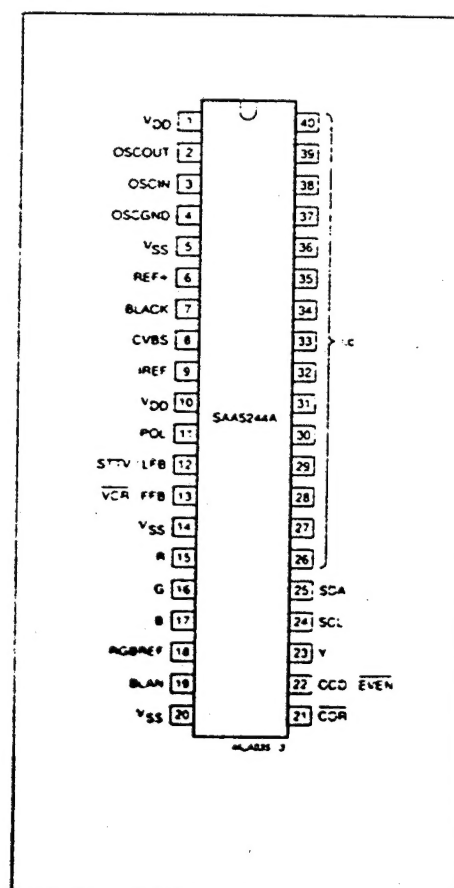


Pin description for TELETEXT SAA 5244A

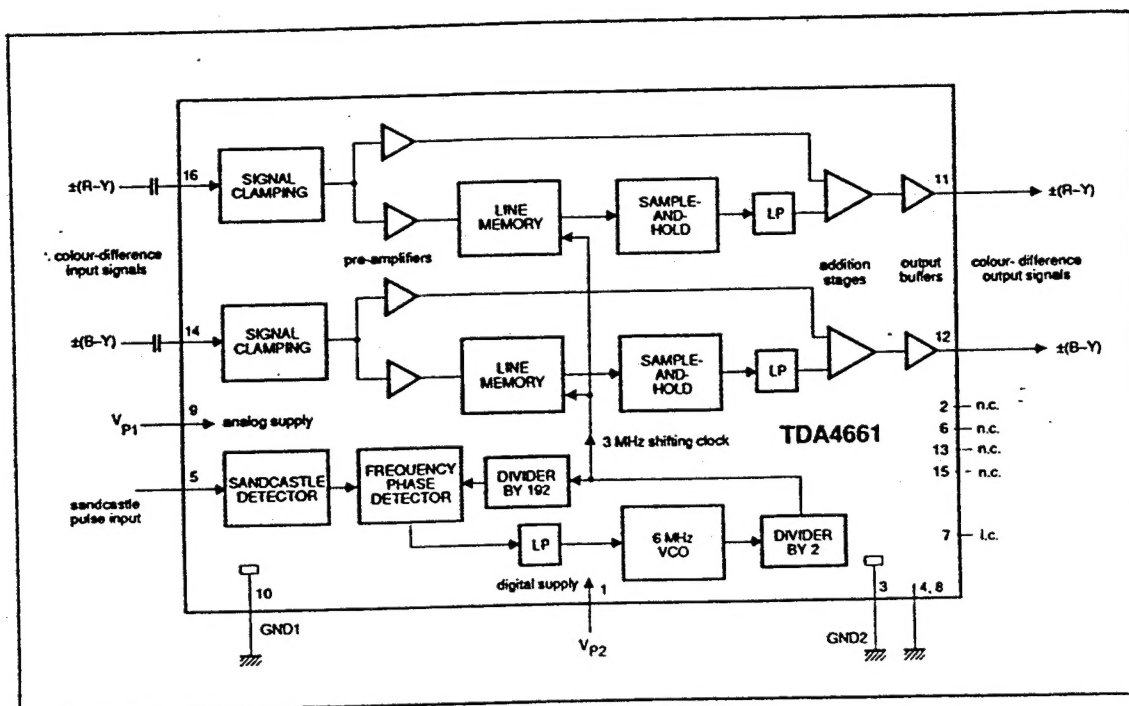
- 1 - +5V power supply
- 2 - 27 MHz oscillator output
- 3 - 27 MHz oscillator input
- 4 - oscillator ground 0 V.
- 5 - ground
- 6 - ADC reference voltage
- 7 - black level reference input
- 8 - composite video input
- 9 - current reference input
- 10 - +5V power supply
- 11 - STTV/LFB/FFB selection
- 12 - sync. input/output
- 13 - PLL time-contrast input
- 14 - ground
- 15 - Red output
- 16 - Green output
- 17 - Blue output
- 18 - dc voltage level on RGB
- 19 - fast blanking output
- 20 - ground
- 21 - contrast-reduction programmable output
- 22 - de-interlace output
- 23 - Y output
- 24 - SCL i2cbus
- 25 - SDA i2cbus
- 26/40 - connected internally

Functional description

The integrated circuit is 625-line single-chip teletext decoder. It combines digital and analog functions and includes a single-page RAM memory.



DELAY LINE - TDA 4661 / TDA 4665



Pinout description

- 1 - digital section +5V power supply
- 2 - not connected
- 3 - digital section ground
- 4 - internally connected
- 5 - sandcastle input
- 6 - not connected
- 7 - internally connected
- 8 - internally connected
- 9 - analog section +5V power supply
- 10 - analog section ground
- 11 - (R-Y) signal output
- 12 - (B-Y) signal output
- 13 - not connected
- 14 - (B-Y) signal input
- 15 - not connected
- 16 - (R-Y) signal input

Functional description

The integrated circuit TDA 4661 is a delay line integrated baseband. It interfaces with decoders with colour difference output signals (R-Y) and (B-Y).